


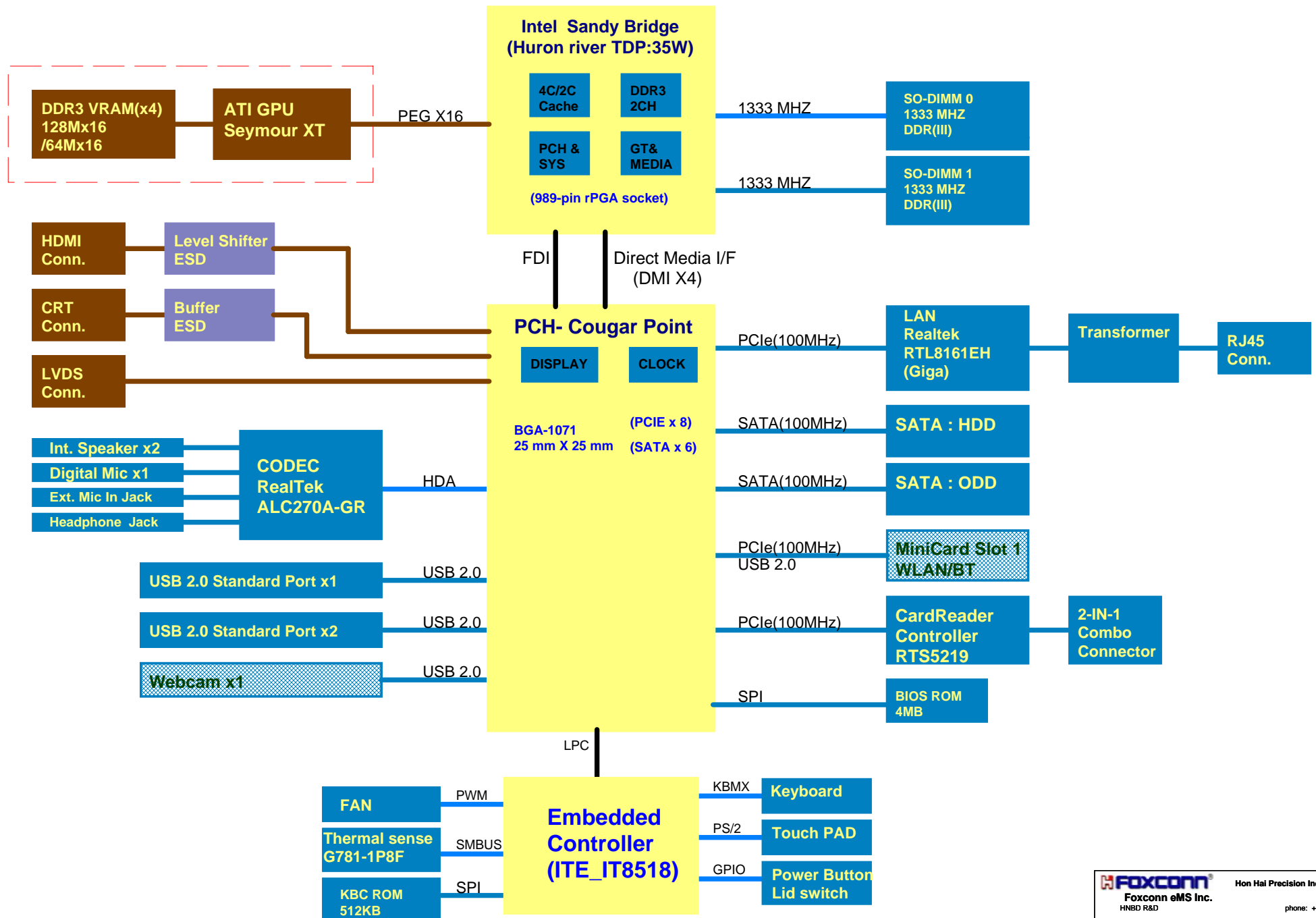
## PROJECT : CHICAGO (For Intel Huron River Platform)

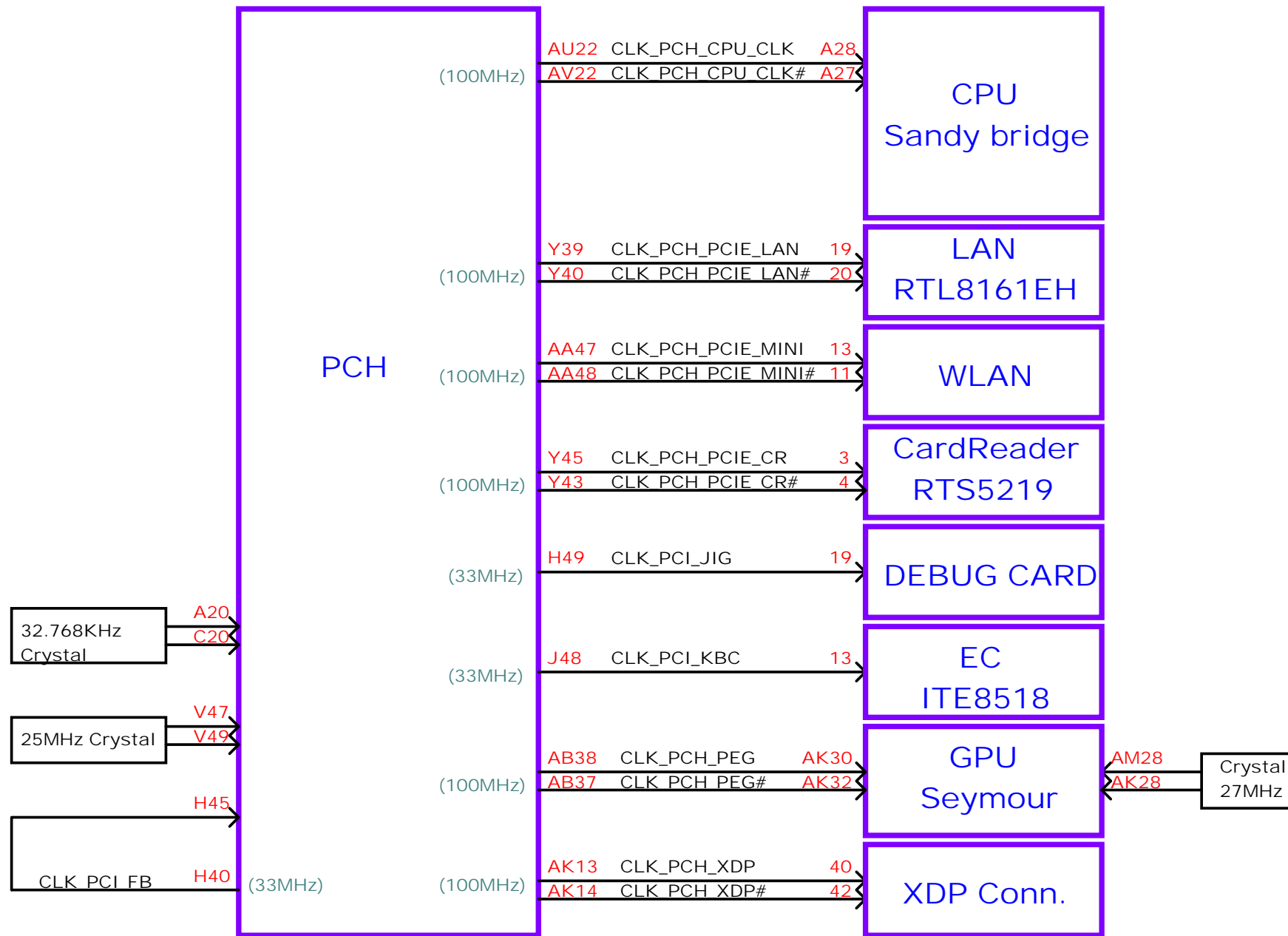
01 -- COVER SHEET	23 -- CougarPoint (HDA, SATA..)
02 -- SYSTEM BLOCK DIAGRAM	24 -- CougarPoint (PCI-E, CLK..)
03 -- CLOCK MAP	25 -- CougarPoint (DMI, FDI..)
04 -- POWER SEQUENCY DIAGRAM	26 -- CougarPoint (USB, GPIO..)
05 -- POWER MAP	27 -- CougarPoint (PWR/GND)
06 -- SMBUS MAP	28 -- CougarPoint (PWR, GND)
07 -- Blank	29 -- DDR3 (SO-DIMM 0&1)
08 -- DCIN/BATT	30 -- VGA (PCI-E/STRAP) 1/3
09 -- PWR_CHARGE	31 -- VGA_S3 (IO) 2/3
10 -- PWR_5V/3.3V	32 -- VGA_S3 (DDR3) 3/3
11 -- PWR_VCCP	33 -- VRAM (DDR3)
12 -- PWR_1.5V/0.75S	34 -- EC+KBC (IT8518) & ROM
13 -- PWR_VCORE	35 -- Audio (CODEC_ALC270A)
14 -- PWR_OTHER	36 -- Audio (JACK+AMP+SPK+Mute)
15 -- PWR_ATVDD	37 -- LAN (RTL8161EH)
16 -- PWR_1.8VS	38 -- Mini PCIe & FAN
17 -- PWR_VCCSA	39 -- USBx2/USB DB/SATA CONN.
18 -- Sandy Bridge (DMI, PEG, FDI)	40 -- Card Reader (RTL5219-GR)
19 -- Sandy Bridge (CLK, JTAG..)	41 -- HDMI & CRT
20 -- Sandy Bridge (DDR3)	42 -- LVDS & Webcam
21 -- Sandy Bridge (PWR/GND)	43 -- Sequence circuit
22 -- Sandy Bridge (GRAPHIC PWR)	

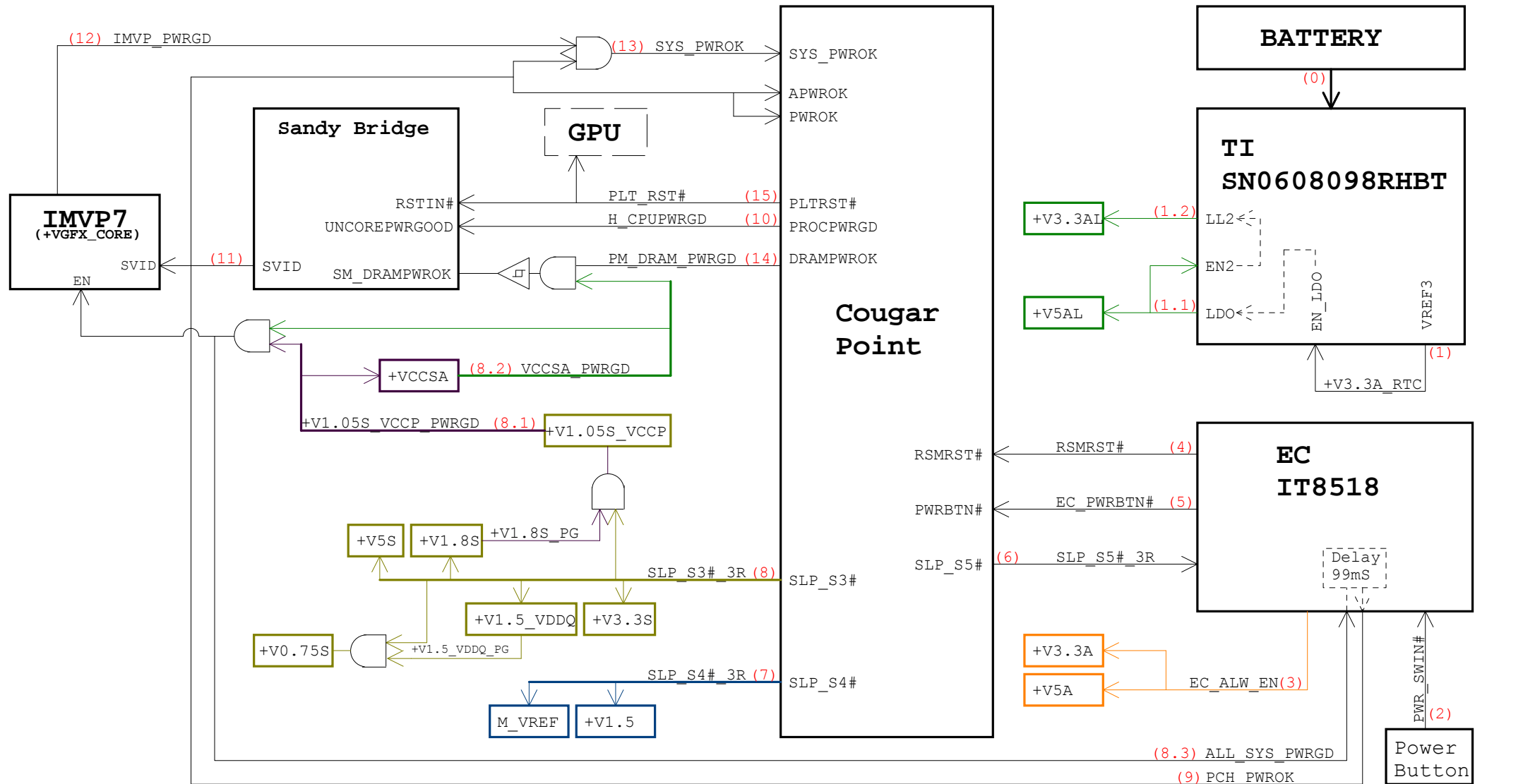
P. Leader	Check by	Design by

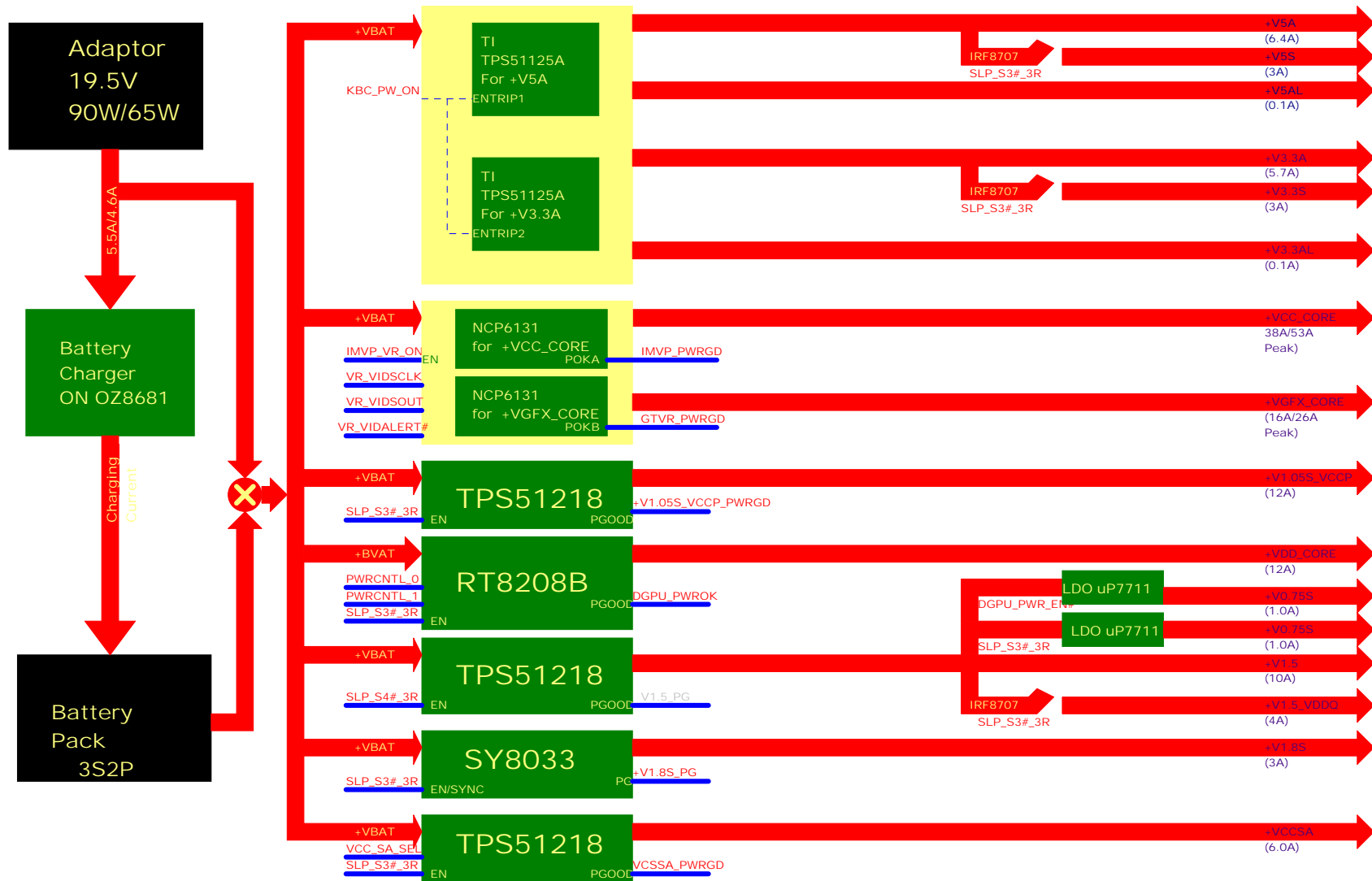
 <b>Foxconn eMS Inc.</b> HNBD R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111
Title		
Index Page		
Size	Document Number	Rev
Custom	CHICAGO	MV
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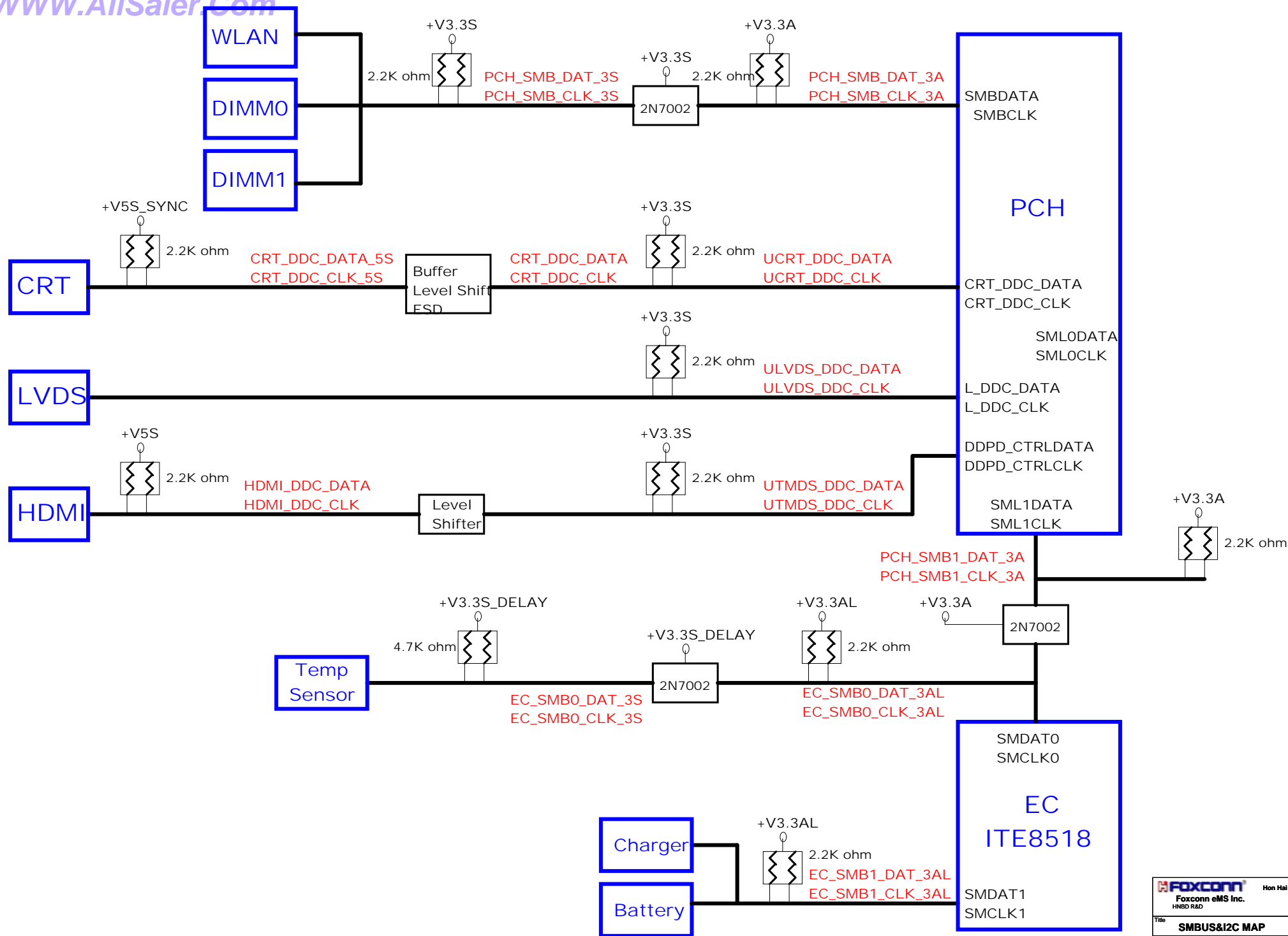


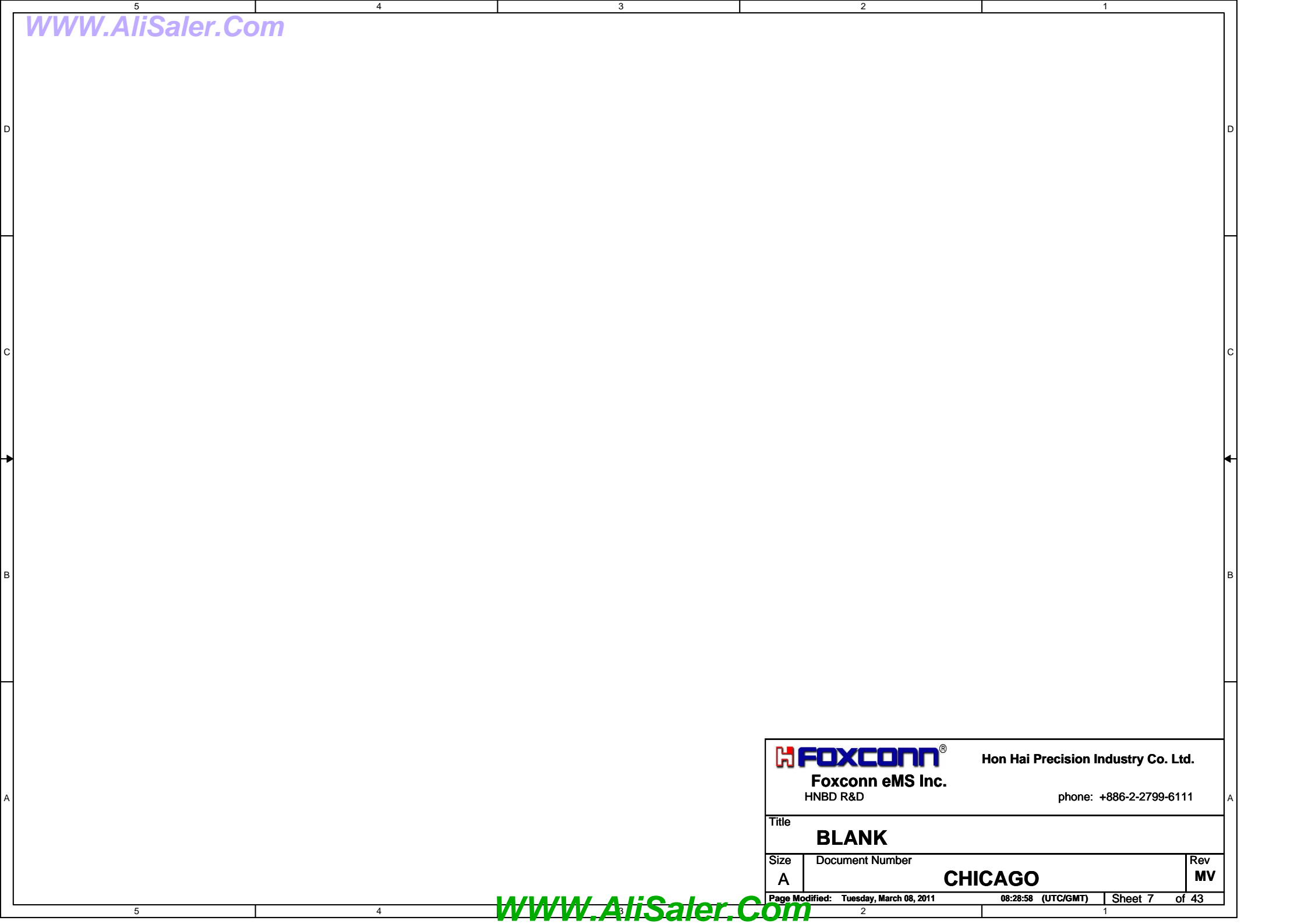




# POWER MAP





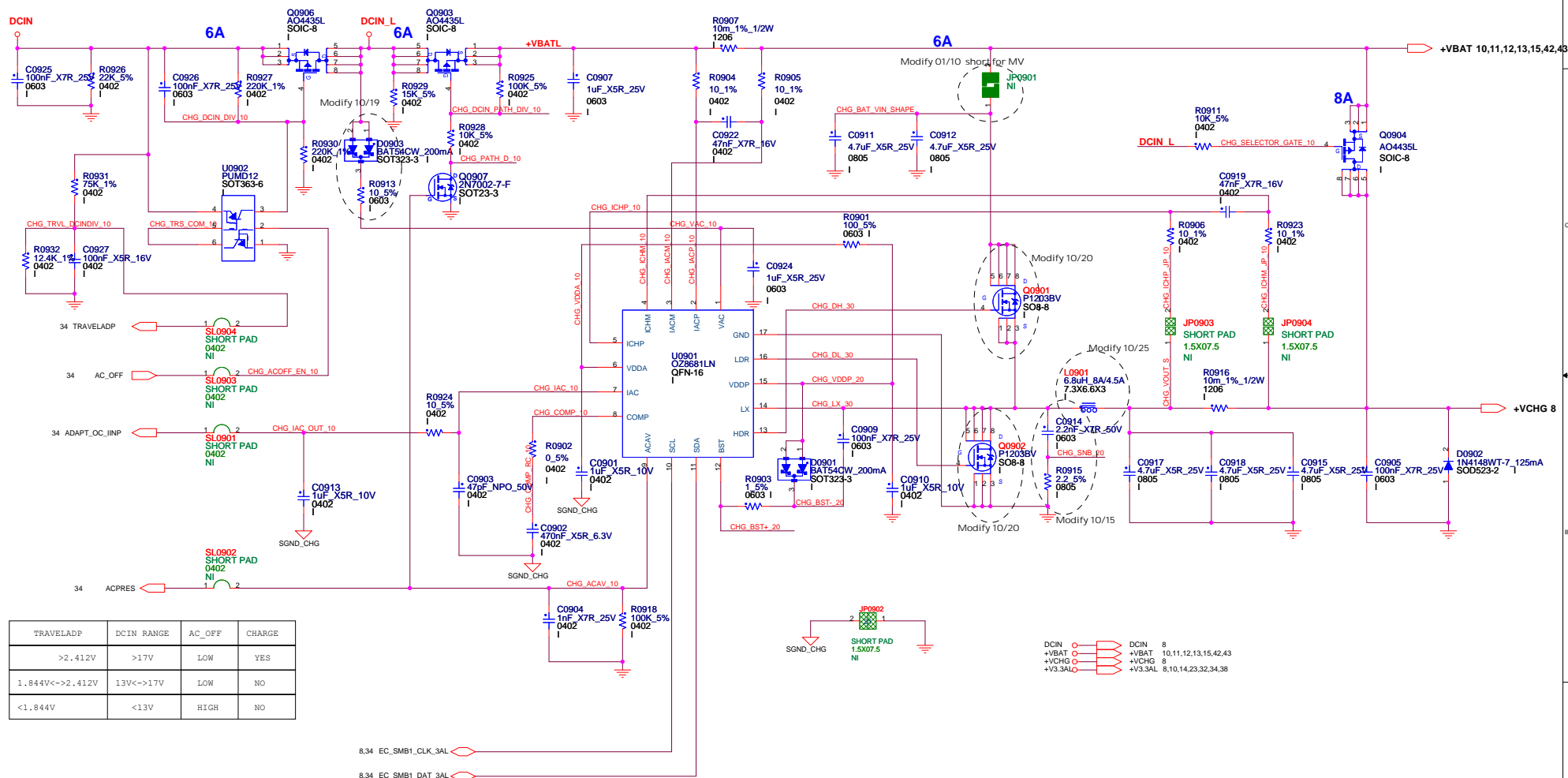


		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		phone: +886-2-2799-6111	
HNBD R&D			
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A	CHICAGO		MV
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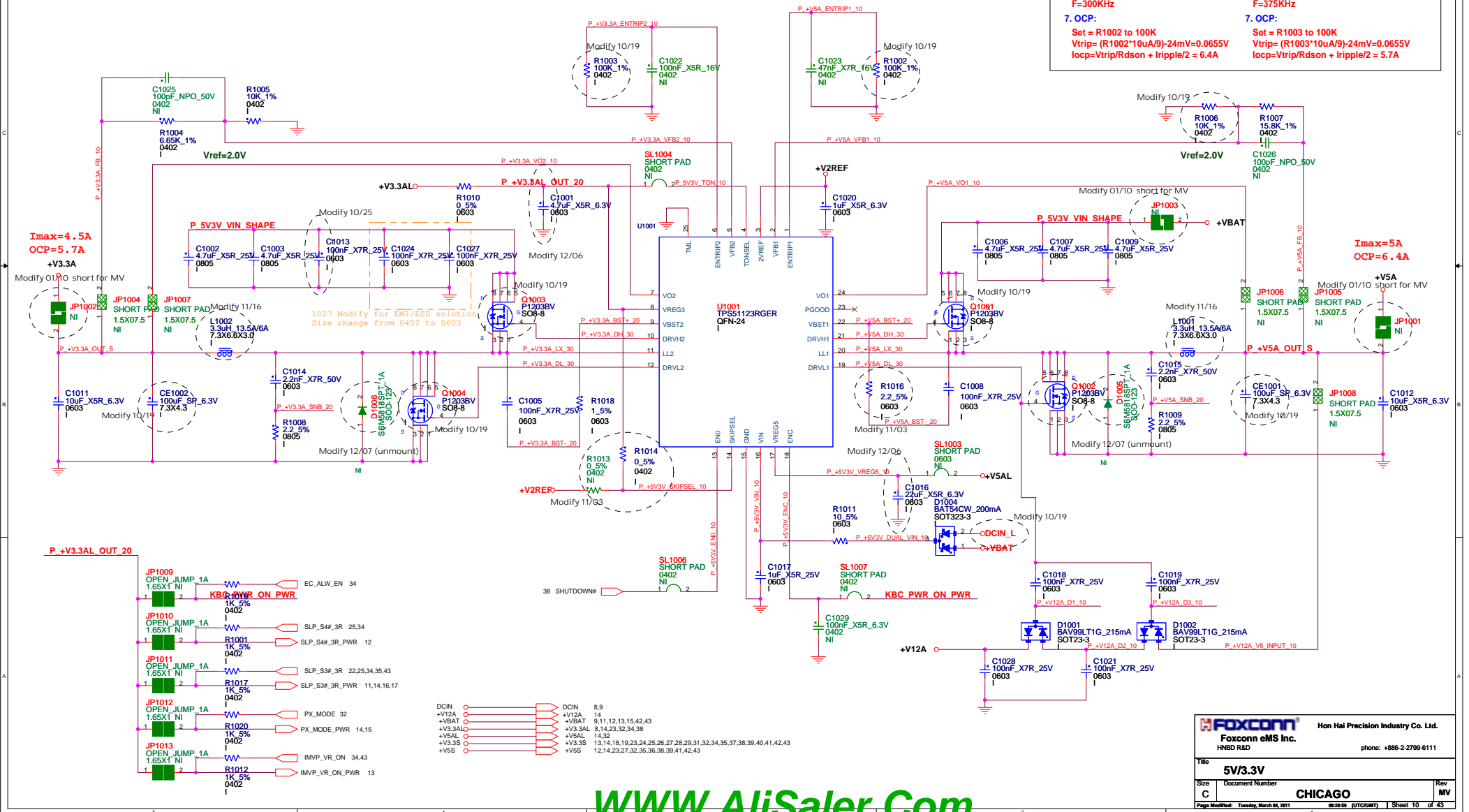
# BATTERY CHARGER



# +V5A / +V3.3A POWER SUPPLY

2010.1103.0

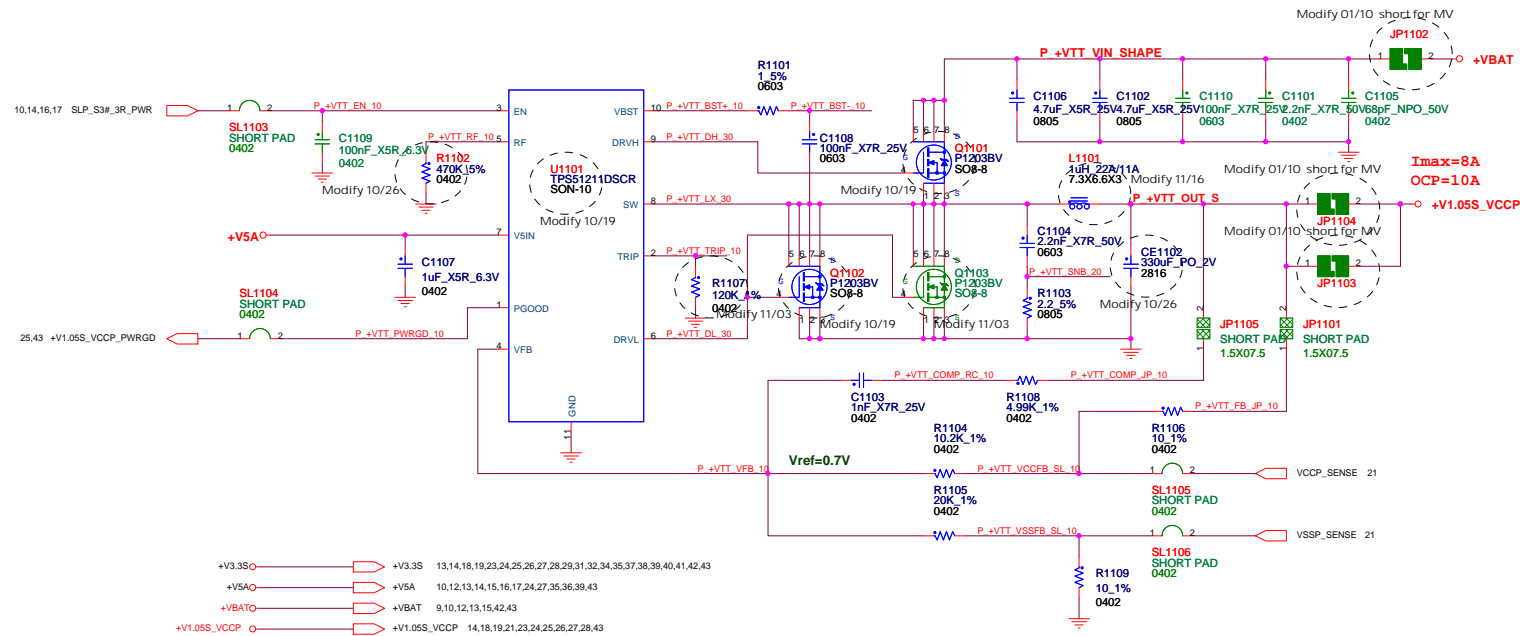
<b>+V5A:</b> 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 3.7A$ 2. Ripple Current: $I_{rip} = 3.72A$ 3. Ripple Voltage: $ESR/1 = 15mohm$ $V_{rip} = 55.8mV$ 4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ 5. MOSFET Spec: H-side MOSFET: IRF8707PBF $R_{ds(ON)} = 17.5mohm$ ( $V_{gs} = 4.5V$ ) $I_{cont} = 11A$ ( $T = 25^\circ C$ ) $I_{peak} = 88A$ (Pause = 10 us) 6. Frequency: $F = 300KHz$ 7. OCP: $Set = R1002 \text{ to } 100K$ $V_{trip} = (R1002 \cdot 10uA/9) - 24mV = 0.0655V$ $I_{ocp} = V_{trip} / R_{dson} + I_{ripple} / 2 = 6.4A$	<b>+V3.3A:</b> 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.2A$ 2. Ripple Current: $I_{rip} = 2.21A$ 3. Ripple Voltage: $ESR/1 = 15mohm$ $V_{rip} = 33.15mV$ 4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ 5. MOSFET Spec: L-side MOSFET: IRF8707PBF $R_{ds(ON)} = 17.5mohm$ ( $V_{gs} = 4.5V$ ) $I_{cont} = 11A$ ( $T = 25^\circ C$ ) $I_{peak} = 88A$ (Pause = 10 us) 6. Frequency: $F = 375KHz$ 7. OCP: $Set = R1003 \text{ to } 100K$ $V_{trip} = (R1003 \cdot 10uA/9) - 24mV = 0.0655V$ $I_{ocp} = V_{trip} / R_{dson} + I_{ripple} / 2 = 5.7A$
---	--



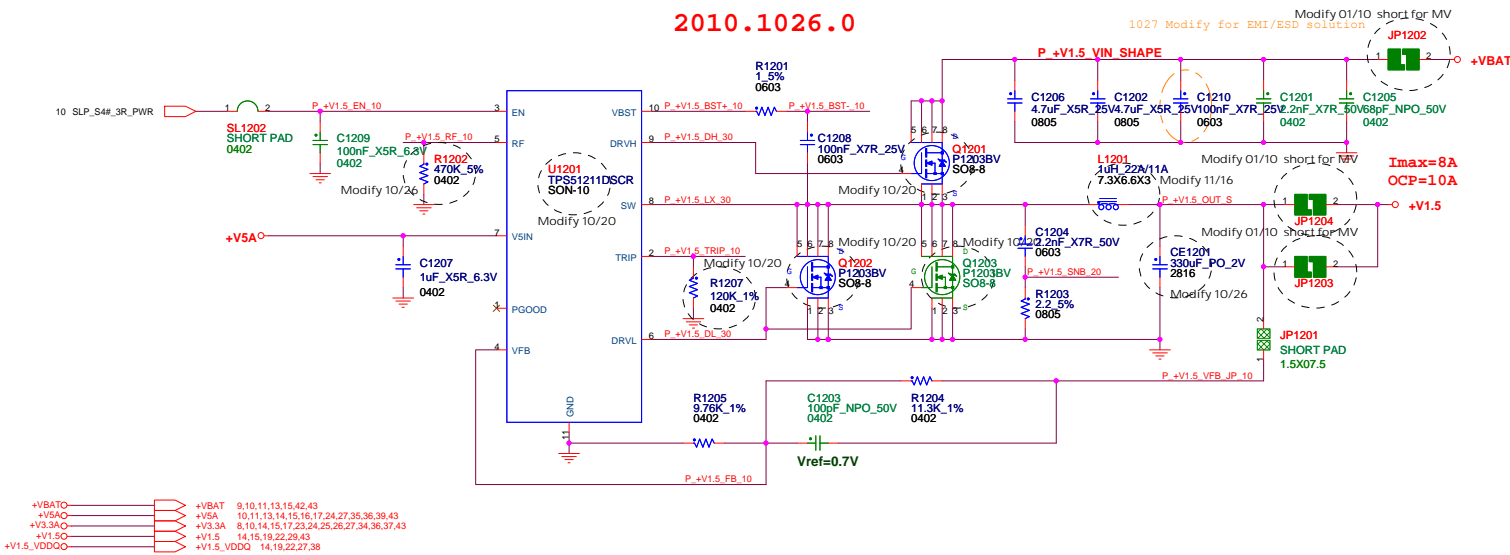
# +VTT POWER SUPPLY

2010.1103.0

- +V1.05S\_VCCP:**
- 1. I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.24A$
  - 2. Ripple Current:**  
 $I_{rip} = 3.42A$
  - 3. Ripple Voltage:**  
 $ESR/1 = 9mohm$   
 $V_{rip} = 30.78mV$
  - 4. Inductor Spec:**  
 $I_{sat} = 36A$   
 $I_{dc} = 18A$   
 $DCR = 3.3mohm$
  - 5. MOSFET Spec:**  
H-side MOSFET: IRF8707PBF  
 $R_{ds(ON)} = 17.5mohm$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 11A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 88A$  (Pause = 10 us)  
L-side MOSFET: IRF8707PBF  
 $R_{ds(ON)} = 17.5mohm$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 11A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 88A$  (Pause = 10 us)
  - 6. Frequency:**  
 $F = 290KHz$  ( $R1102 = 0ohm$ )
  - 7. OCP:**  
Set = R1107 to 120K  
 $V_{trip} = R1107 \cdot 10uA = 1.2V$   
 $I_{ocp} = (V_{trip} / 8 \cdot R_{ds(on)}) + I_{ripple} / 2 = 10A$



2010.1026.0



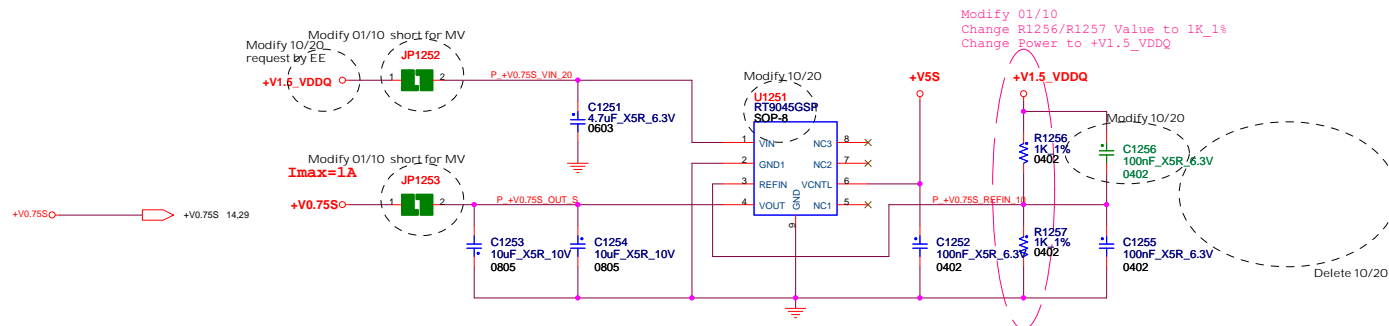
- ```

+V1:
1. VP Current:
  Iin=Vo*Io/(0.75*Vin)=1.78A
2. Ripple Current:
  Irip=3.34A
3. Ripple Voltage:
  ESR/I=9mohm
  Vrip=30.6mV
4. Inductor Spec:
  Isat=36A
  Idc=18A
  DCR=3.3mohm
5. MOSFET Spec:
  H-side MOSFET: IRF8707PBF      L-side MOSFET: IRF8707PBF
  Rds(ON)=17.5mohm (Vgs=4.5 V)    Rds(ON)=17.5mohm (Vgs=4.5 V)
  I cont = 11A (T ~25 °C)          I cont = 11A (T ~25 °C)
  I peak = 88A (Pause =40 us)       I peak = 88A (Pause =40 us)
6. Frequency:
  F=290KHz (R0902=0ohm)
7. OCP:
  Set = R1207 to 120K
  Vtrip= R1207*10uA=1.2V
  Iocp=(Vtrip/8*Rdson) + Iripple/2 = 10A

```

## +V0.75S POWER SUPPLY

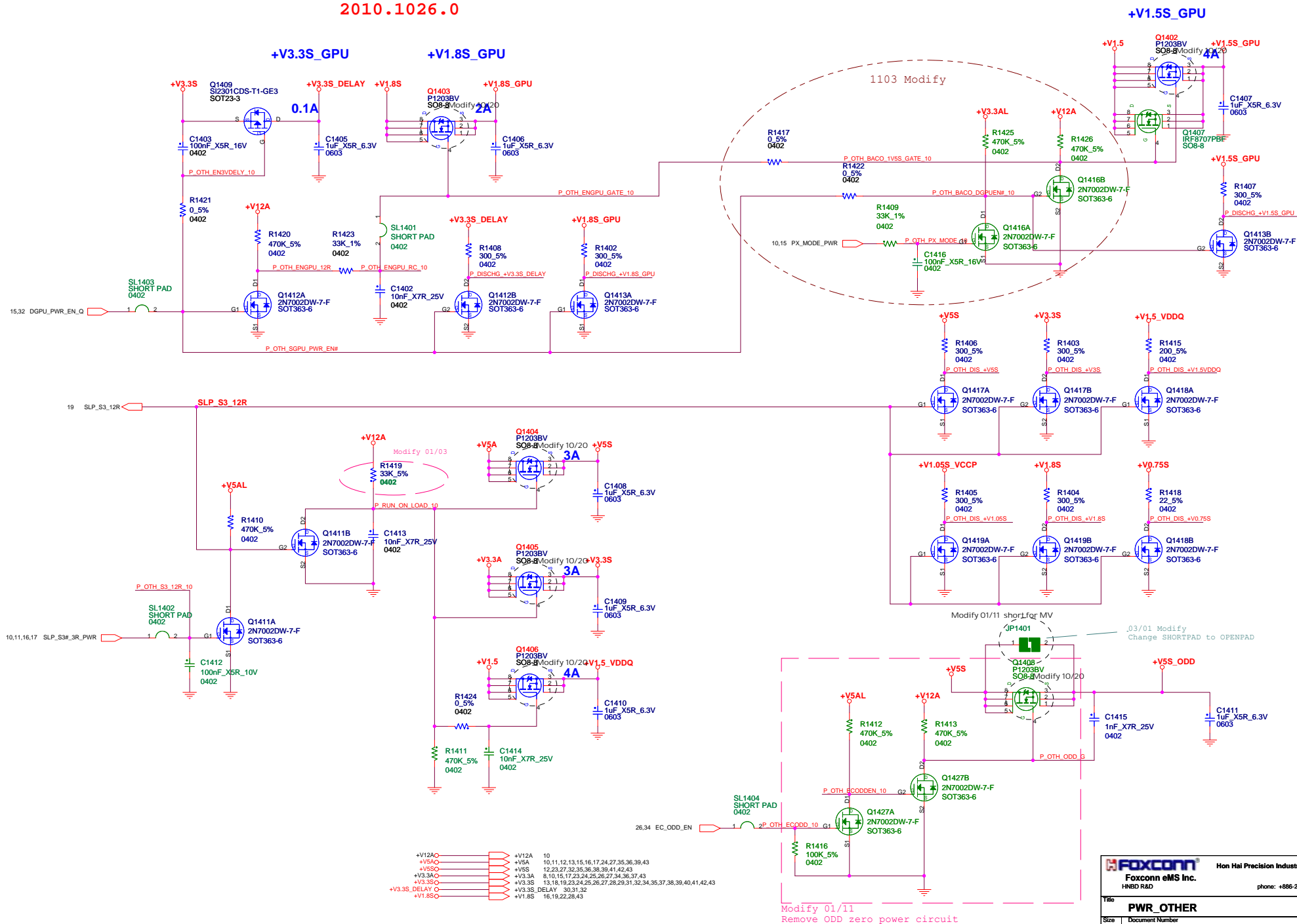
2010.1026.0



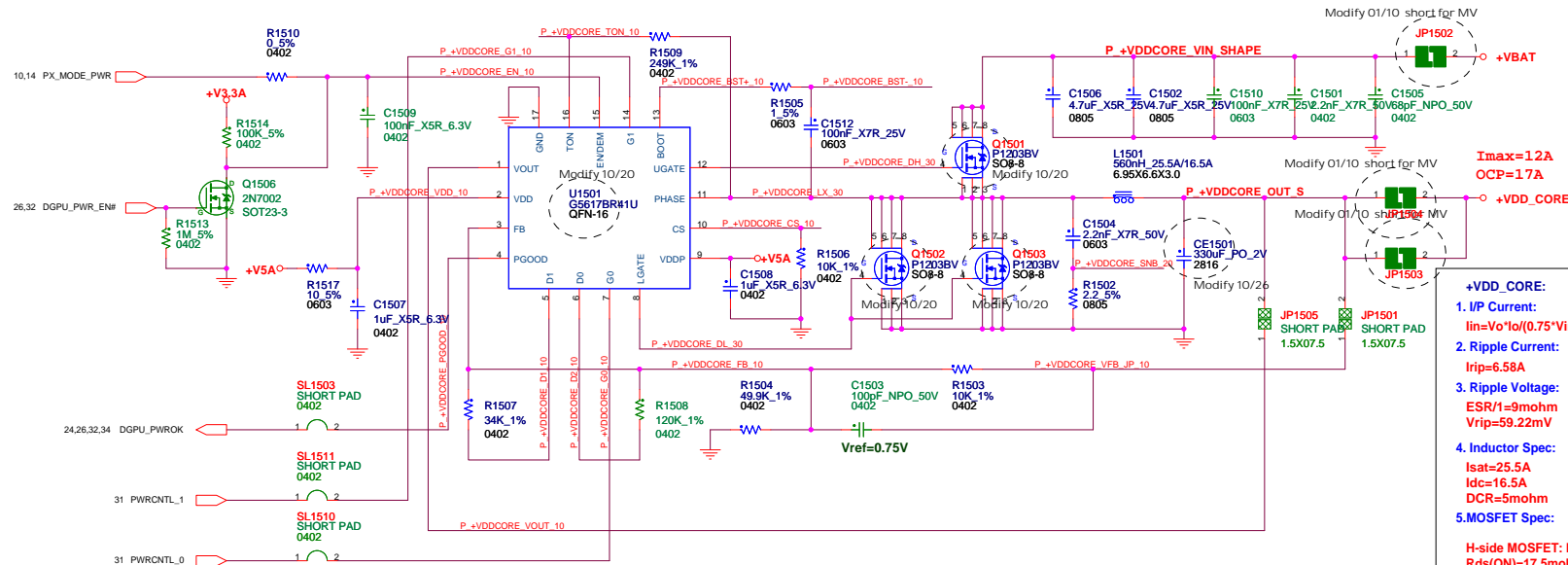
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2010.1026.0



2010.1026.0

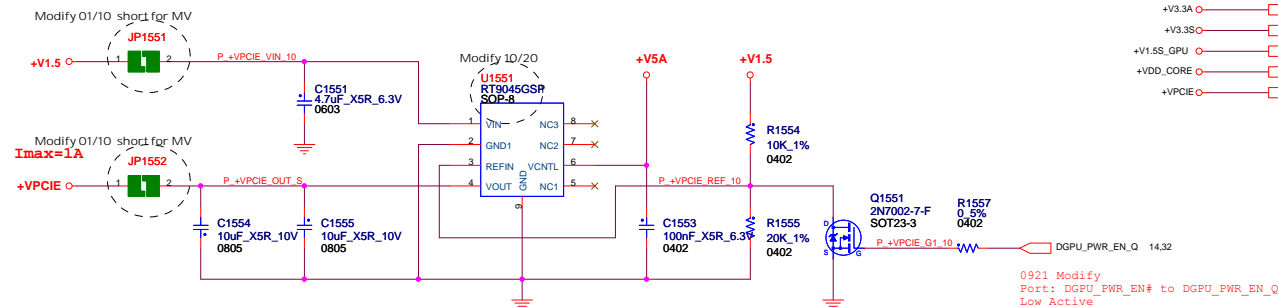


| PWRCNTL_1 | PWRCNTL_0 | VDD_CORE |
|-----------|-----------|----------|
| 0         | ---       | 1.121V   |
| ---       | ---       | ---      |
| 1         | ---       | 0.9V     |
| ---       | ---       | ---      |

**+VDD\_CORE:**

1. **IP Current:**  
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.48A$
2. **Ripple Current:**  
 $I_{rip} = 6.58A$
3. **Ripple Voltage:**  
 $ESR / f = 9m\Omega$   
 $V_{rip} = 59.22mV$
4. **Inductor Spec:**  
 $I_{sat} = 25.5A$   
 $I_{dc} = 16.5A$   
 $DCR = 5m\Omega$
5. **MOSFET Spec:**
- |                                                |                                                |
|------------------------------------------------|------------------------------------------------|
| H-side MOSFET: IRF8707PBF                      | L-side MOSFET: IRF8707PBF                      |
| $R_{ds(ON)} = 17.5m\Omega$ ( $V_{gs} = 4.5V$ ) | $R_{ds(ON)} = 17.5m\Omega$ ( $V_{gs} = 4.5V$ ) |
| $I_{cont} = 11A$ ( $T = 25^\circ C$ )          | $I_{cont} = 11A$ ( $T = 25^\circ C$ )          |
| $I_{peak} = 88A$ (Pause = 10 us)               | $I_{peak} = 88A$ (Pause = 10 us)               |
6. **Frequency:**  
 $T_{ON} = 9.6 \cdot P \cdot R_{1509} \cdot (V_{OUT} + 0.1) / (V_{IN} - 0.3) + 50ns = 206ns$   
 $F = V_{OUT} / (V_{IN} \cdot T_{ON}) = 286KHz$
7. **OCp:**  
 $Set = R_{1506} \cdot 10K$   
 $V_{trip} = R_{1206} \cdot 10uA = 0.1V$   
 $I_{ocp} = (V_{trip} / R_{ds(on)}) + I_{ripple} / 2 = 17A$

## 2010.1020.0 +VPCIE POWER SUPPLY



|            |                                                                                       |            |                                                                   |
|------------|---------------------------------------------------------------------------------------|------------|-------------------------------------------------------------------|
| +VBAT      |  | +VBAT      | 9,10,11,12,13,42,43                                               |
| +V5A       |  | +V5A       | 10,11,12,13,14,16,17,24,27,35,36,39,43                            |
| +V3.3A     |  | +V3.3A     | 8,10,14,17,23,24,25,26,27,34,36,37,43                             |
| +V3.3S     |  | +V3.3S     | 13,14,18,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43 |
| +V1.5S_GPU |  | +V1.5S_GPU | 14,30,32,33,43                                                    |
| +VDD_CORE  |  | +VDD_CORE  | 32,43                                                             |
| +VPCIE     |  | +VPCIE     | 30,31,32,43                                                       |

```
0921 Modify
Port: DGPU_PWR_EN# to DGPU_PWR_EN_Q
Low Active
```

# +V1.8S POWER SUPPLY

2010.1025.0

+V1.8S:

1. I/P Current:

$$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.44A$$

2. Ripple Current:

$$I_{rip} = 0.53A$$

3. Ripple Voltage:

$$ESR/3 = 3.3m\Omega$$

$$V_{rip} = 1.75mV$$

4. Inductor Spec:

$$I_{sat} = 14A$$

$$I_{dc} = 8A$$

$$DCR = 20m\Omega$$

5. MOSFET Spec:

H-side P-MOSFET:

L-side N-MOSFET:

$$R_{ds(ON)} = 110m\Omega \quad (V_{gs} = 4.5V)$$

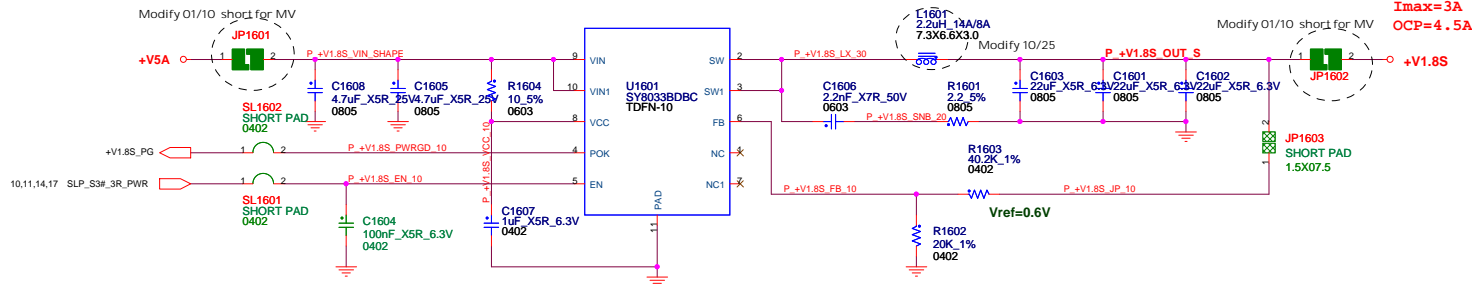
$$R_{ds(ON)} = 75m\Omega \quad (V_{gs} = 4.5V)$$

6. Frequency:

$$F = 1MHz \quad (\min = 800KHz, \max = 1.2MHz)$$

7. OCP:

$$I_{ocp} = 4A(\min) / 4.5A(\text{typ}) / 5A(\max)$$



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Title

+1.8VS

Size

Document Number

CHICAGO

Rev

MV

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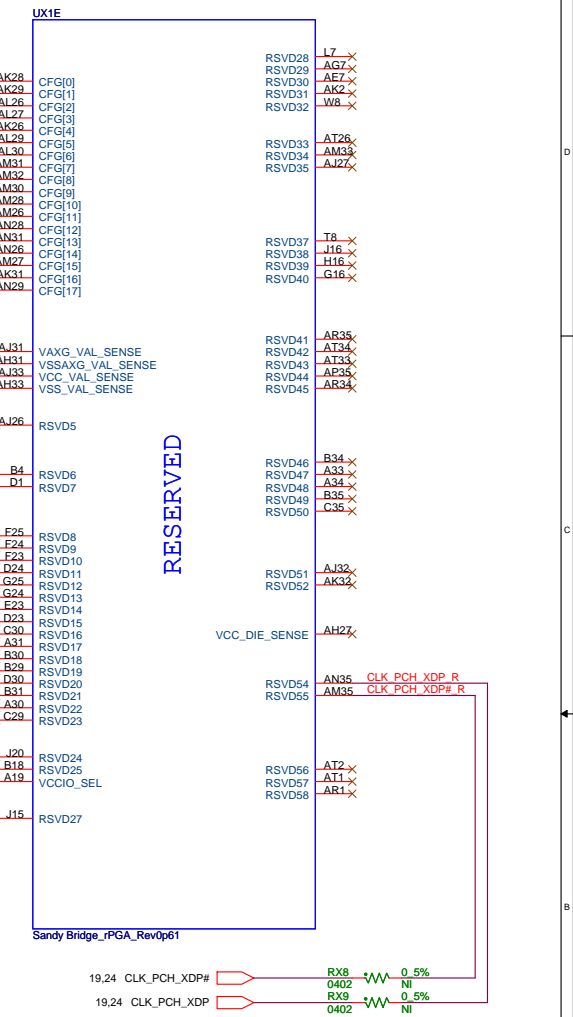
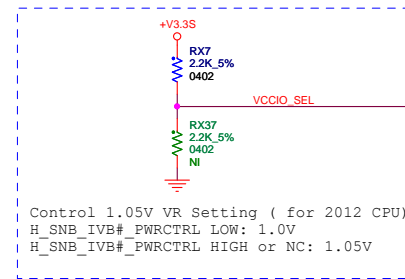
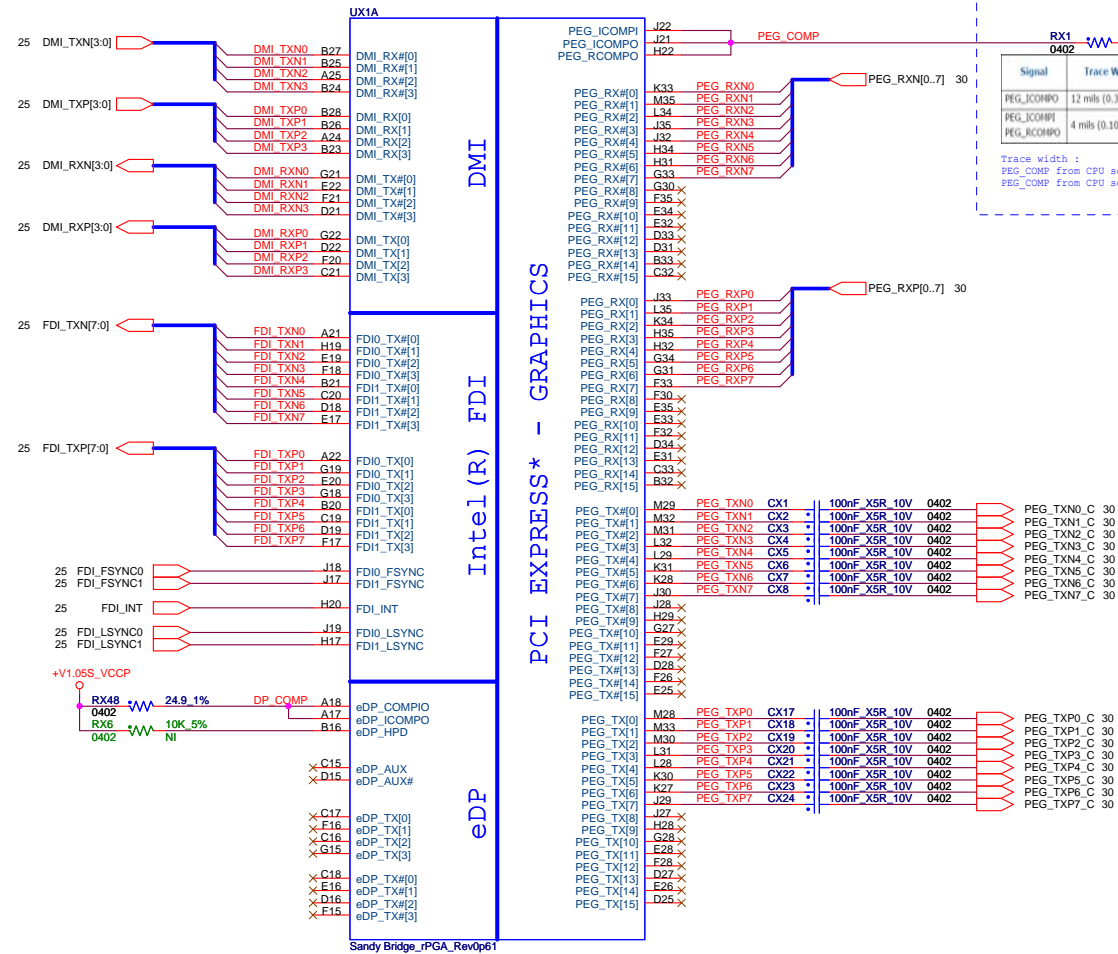
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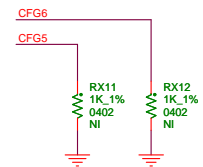


+V3.3S 13,14,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43  
+V1.05S\_VCCP 11,14,19,21,23,24,25,26,27,28,43



CFG4 Display Port Presence Strap  
CFG4 1:(Default) Disabled/No Physical Display Port attached to Embedded Display Port  
0:Enabled;An external Display Port is connect to Embedded Display Port

CFG7 PEG DEFER TRAINING  
CFG7 1:(Default) PEG Train immediately following xxRESETB de assertion  
0:PEG Wait for BIOS for training



PCIE Port Bifurcation Straps  
CFG[6:5] 11:(Default) x16 - Device 1 functions & 2 disabled  
10:x8,x8 - Device 1 function 1 enabled ; function 2 disabled  
01:Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
00:x8,x4,x4 - (Device 1 functions 1 & 2 enabled)

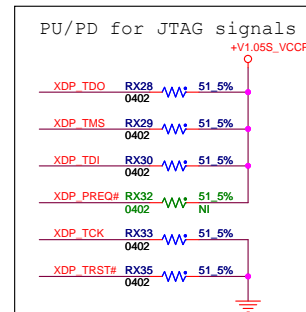
PEG Static Lane Reversal - CFG2 is for the 16x  
CFG2 1:(Default) Normal Operation;Lane # definition matches socket pin map definition  
0:Lane Reversed

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HNB2 R&D  
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Title: **PROCESSOR(1 of 5)**

Size: Document Number  
Custom **CHICAGO** Rev **MV**

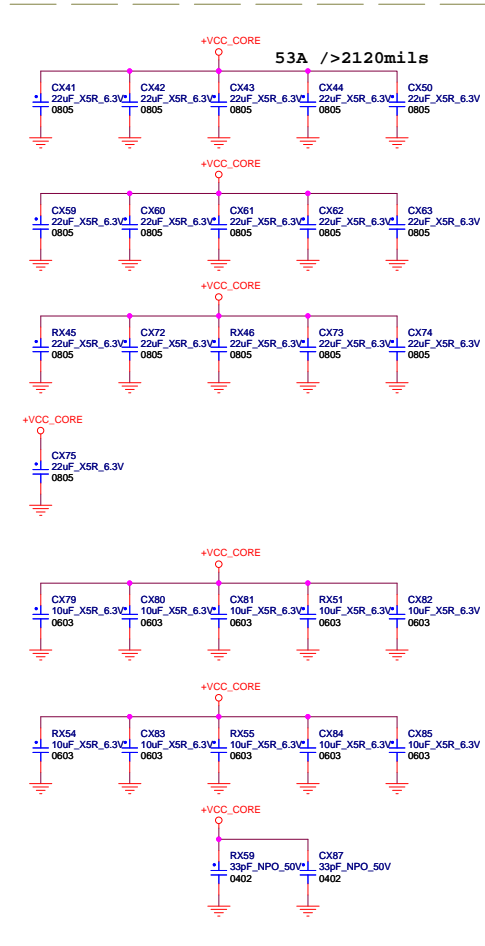
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+V1.05S\_VCCP 11,14,18,19,23,24,25,26,27,28,43  
+VCC\_CORE 13,18,43

FOR VCC:  
4x 330  $\mu$ F Bottom Edge,  
10x 0603 10  $\mu$ F Bottom Cavity,  
8x 0805 22  $\mu$ F Top Cavity,  
8x 0805 22  $\mu$ F Top Edge,



- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AD36 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC36 VCC31
- AC35 VCC32
- AC34 VCC33
- AC33 VCC34
- AC32 VCC35
- AC31 VCC36
- AC30 VCC37
- AC29 VCC38
- AC28 VCC39
- AC27 VCC40
- AC26 VCC41
- AC25 VCC42
- AA34 VCC43
- AA33 VCC44
- AA32 VCC45
- AA31 VCC46
- AA30 VCC47
- AA29 VCC48
- AA28 VCC49
- AA27 VCC50
- AA26 VCC51
- Y35 VCC52
- Y34 VCC53
- Y33 VCC54
- Y32 VCC55
- Y31 VCC56
- Y30 VCC57
- Y29 VCC58
- Y28 VCC59
- Y27 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- V26 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- U26 VCC80
- R35 VCC81
- R34 VCC82
- R33 VCC83
- R32 VCC84
- R31 VCC85
- R30 VCC86
- R29 VCC87
- R28 VCC88
- R27 VCC89
- R26 VCC90
- P35 VCC91
- P34 VCC92
- P33 VCC93
- P32 VCC94
- P31 VCC95
- P30 VCC96
- P29 VCC97
- P28 VCC98
- P27 VCC99
- P26 VCC100

Sandy Bridge\_rPGA\_Rev0p61

## POWER

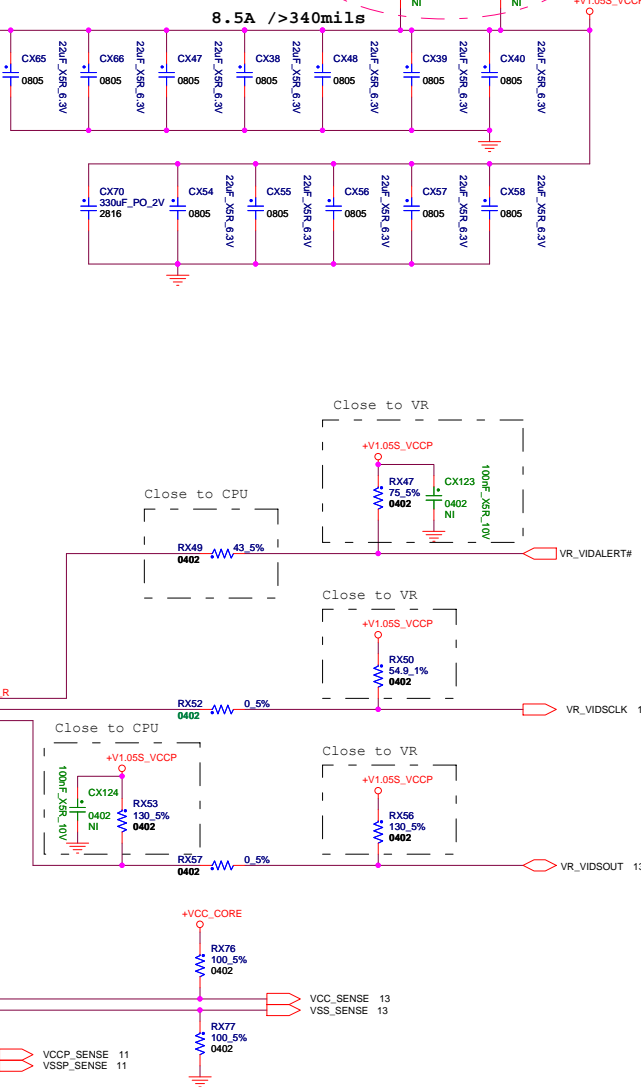
### PEG AND DDR

### CORE SUPPLY

### SVID

### SENSE LINES

FOR VCCIO:  
2x 330  $\mu$ F,  
5x 0805 22  $\mu$ F Bottom Cavity,  
7x 0805 22  $\mu$ F Top Cavity,

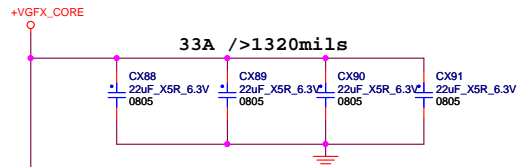


- AT36 VSS1
- AT35 VSS2
- AT34 VSS3
- AT33 VSS4
- AT32 VSS5
- AT31 VSS6
- AT30 VSS7
- AT29 VSS8
- AT28 VSS9
- AT27 VSS10
- AT26 VSS11
- AT25 VSS12
- AT24 VSS13
- AT23 VSS14
- AT22 VSS15
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- AT01 VSS147
- AT00 VSS148
- AT36 VSS149
- AT35 VSS150
- AT34 VSS151
- AT33 VSS152
- AT32 VSS153
- AT31 VSS154
- AT30 VSS155
- AT29 VSS156
- AT28 VSS157
- AT27 VSS158
- AT26 VSS159
- AT25 VSS160
- AT24 VSS161
- AT23 VSS162
- AT22 VSS163
- AT21 VSS164
- AT20 VSS165
- AT19 VSS166
- AT18 VSS167
- AT17 VSS168
- AT16 VSS169
- AT15 VSS170
- AT14 VSS171
- AT13 VSS172
- AT12 VSS173
- AT11 VSS174
- AT10 VSS175
- AT09 VSS176
- AT08 VSS177
- AT07 VSS178
- AT06 VSS179
- AT05 VSS180
- AT04 VSS181
- AT03 VSS182
- AT02 VSS183
- AT01 VSS184
- AT00 VSS185

Sandy Bridge\_rPGA\_Rev0p61

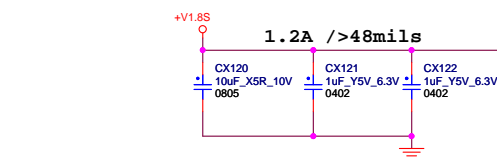
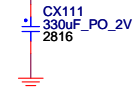
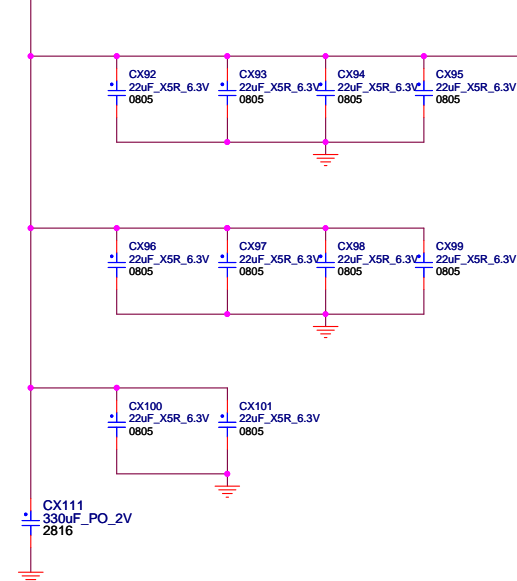
**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
Foxconn eMS Inc.  
HNBD R&D phone: +886-2-2799-6111

Title: **PROCESSOR(4 of 5)**  
Size: Document Number  
Custom: **CHICAGO** Rev: MV  
Page Modified: Tuesday, March 06, 2011 08:28:46 (UTC+8) Sheet 21 of 43

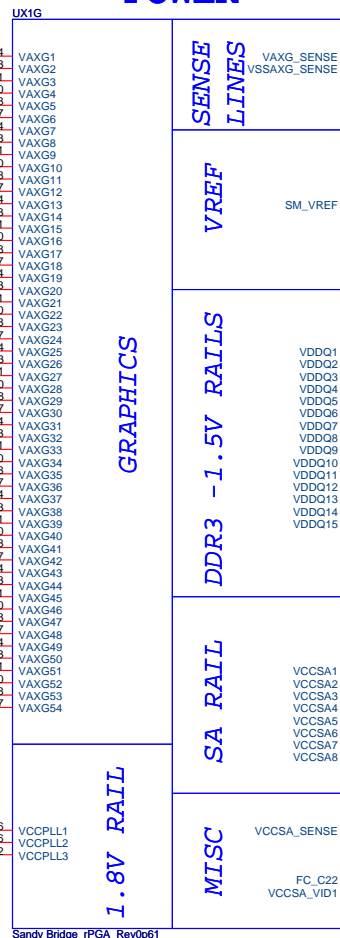


FOR VAXG:  
2x 330  $\mu$ F Bottom Edge,  
4x 0805 22  $\mu$ F Top & Bottom Cavity,  
8x 0805 22  $\mu$ F Top & Bottom Edge,

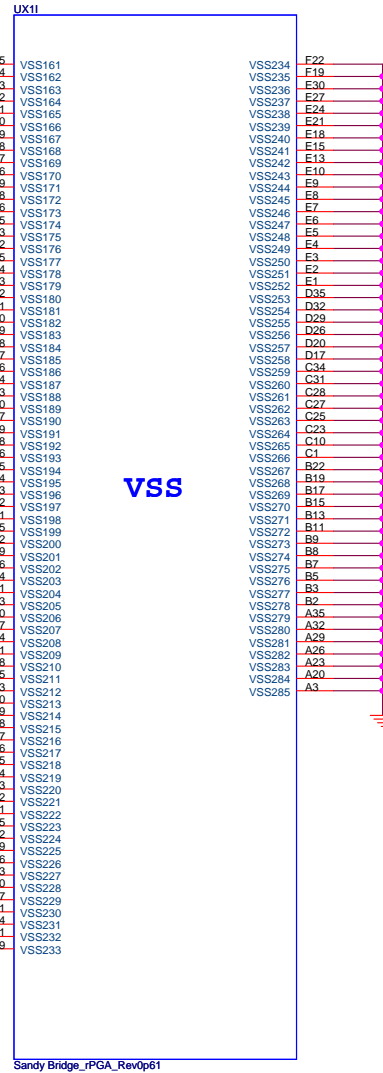
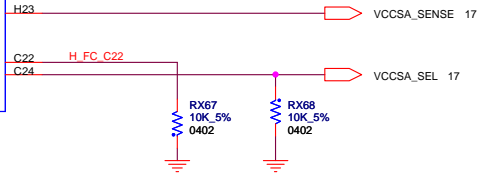
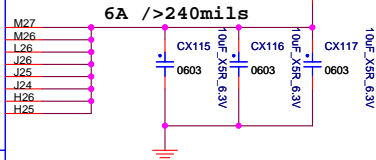
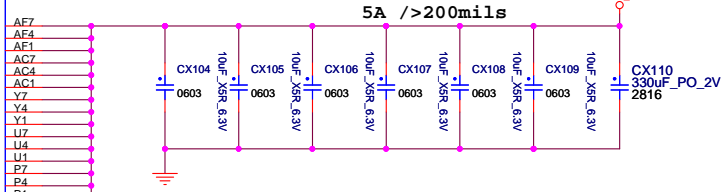
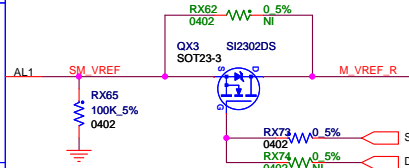
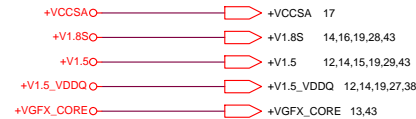
## POWER



FOR VCCPLL:  
1x 330  $\mu$ F Bottom Edge,  
2x 0402 1  $\mu$ F Bottom Edge,  
1x 0805 10  $\mu$ F Bottom Edge,

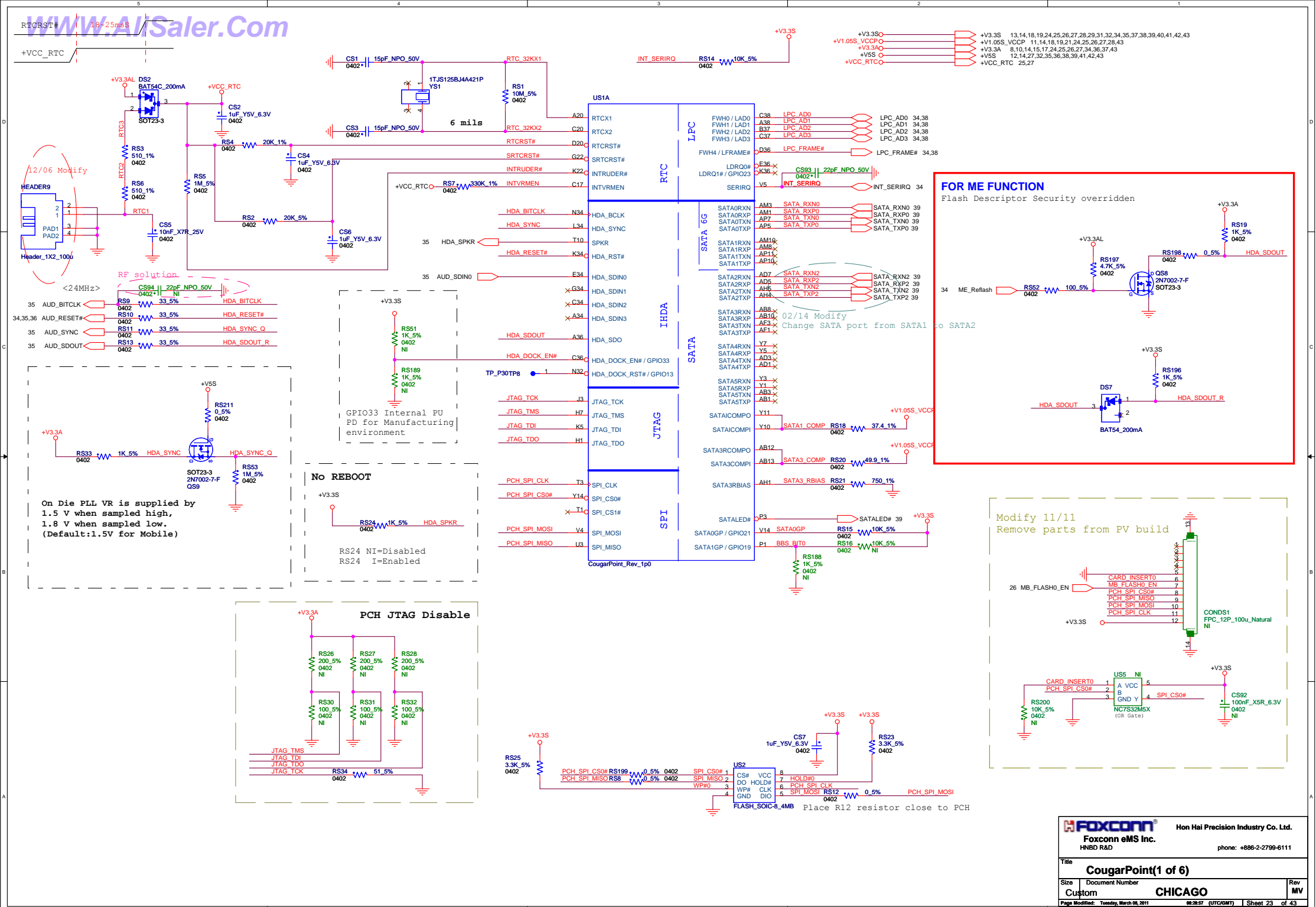


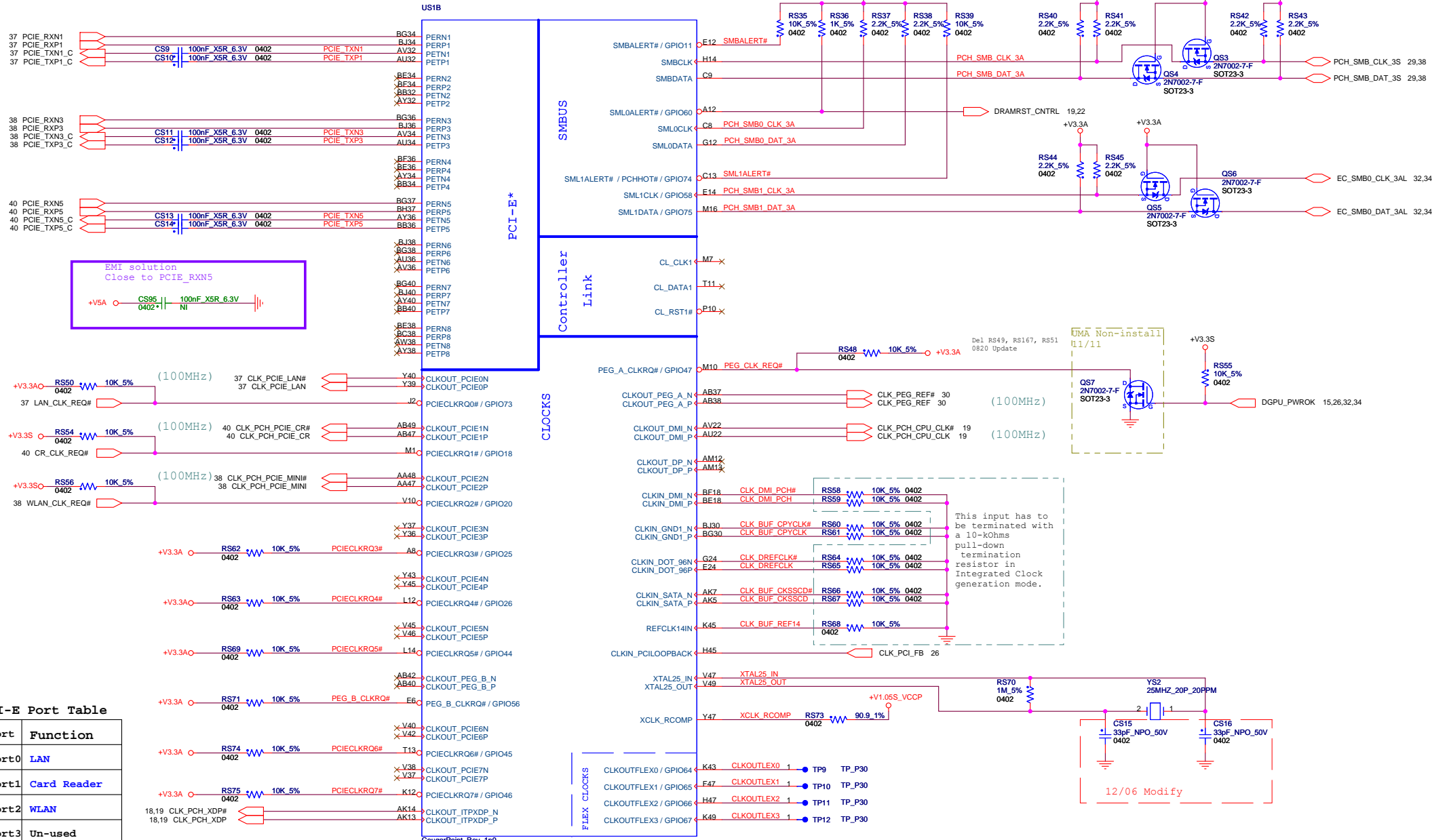
Sandy Bridge\_rPGA\_Rev0p61



Sandy Bridge\_rPGA\_Rev0p61







| Port  | Function    |
|-------|-------------|
| Port0 | LAN         |
| Port1 | Card Reader |
| Port2 | WLAN        |
| Port3 | Un-used     |
| Port4 | Un-used     |
| Port5 | Un-used     |
| Port6 | Un-used     |
| Port7 | Un-used     |

| Port  | Function    |
|-------|-------------|
| Port0 | LAN         |
| Port1 | Card Reader |
| Port2 | WLAN        |
| Port3 | Un-used     |
| Port4 | Un-used     |
| Port5 | Un-used     |
| Port6 | Un-used     |
| Port7 | Un-used     |



US1C

US1D

US1E

US1F

US1G

US1H

US1I

US1J

US1K

US1L

US1M

US1N

US1O

US1P

US1Q

US1R

US1S

US1T

US1U

US1V

US1W

US1X

US1Y

US1Z

US1AA

US1AB

US1AC

US1AD

US1AE

US1AF

US1AG

US1AH

US1AI

US1AJ

US1AK

US1AL

US1AM

US1AN

US1AO

US1AP

US1AQ

US1AR

US1AS

US1AT

US1AU

US1AV

US1AW

US1AX

US1AY

US1AZ

US1BA

US1BB

US1BC

US1BD

US1BE

US1BF

US1BG

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US1BI

US1BJ

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US1BL

US1BM

US1BN

US1BO

US1BP

US1BQ

US1BR

US1BS

US1BT

US1BU

US1BV

US1BW

US1BX

US1BY

US1BZ

US1CA

US1CB

US1CC

US1CD

US1CE

US1CF

US1CG

US1CH

US1CI

US1CJ

US1CK

US1CL

US1CM

US1CN

US1CO

US1CP

US1CQ

US1CR

US1CS

US1CT

US1CU

US1CV

US1CW

US1CX

US1CY

US1CZ

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US1DY

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US1EB

US1EC

US1ED

US1EE

US1EF

US1EG

US1EH

US1EI

US1EJ

US1EK

US1EL

US1EM

US1EN

US1EO

US1EP

US1EQ

US1ER

US1ES

US1ET

US1EU

US1EV

US1EW

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US1EY

US1EZ

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US1FQ

US1FR

US1FS

US1FT

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US1GY

US1GZ

US1HA

US1HB

US1HC

US1HD

US1HE

US1HF

US1HG

US1HH

US1HI

US1HJ

US1HK

US1HL

US1HM

US1HN

US1HO

US1HP

US1HQ

US1HR

US1HS

US1HT

US1HU

US1HV

US1HW

US1HX

US1HY

US1HZ

US1IA

US1IB

US1IC

US1ID

US1IE

US1IF

US1IG

US1IH

US1II

US1IJ

US1IK

US1IL

US1IM

US1IN

US1IO

US1IP

US1IQ

US1IR

US1IS

US1IT

US1IU

US1IV

US1IW

US1IX

US1IY

US1IZ

US1JA

US1JB

US1JC

US1JD

US1JE

US1JF

US1JG

US1JH

US1JI

US1JJ

US1JK

US1JL

US1JM

US1JN

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US1JV

US1JW

US1JX

US1JY

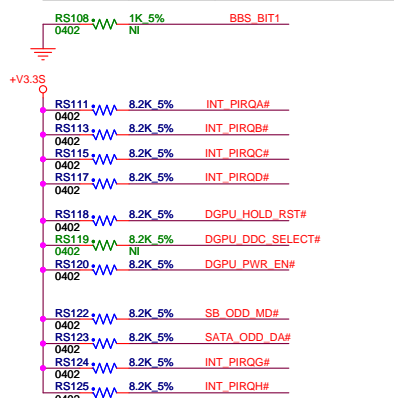
US1JZ

US1KA

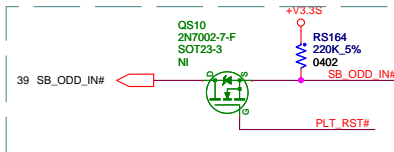
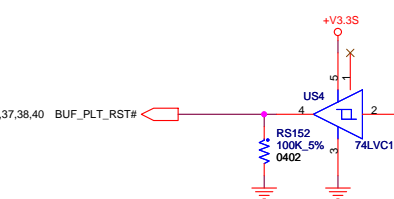
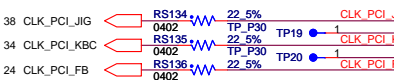
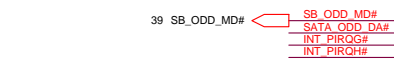
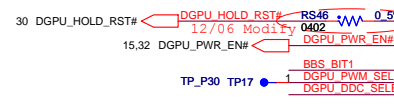
US1KB

US1KC

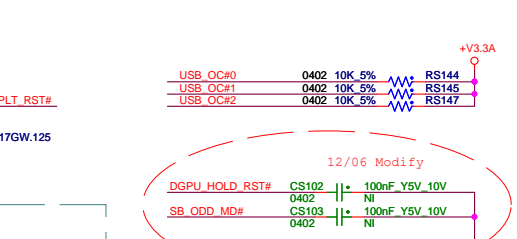
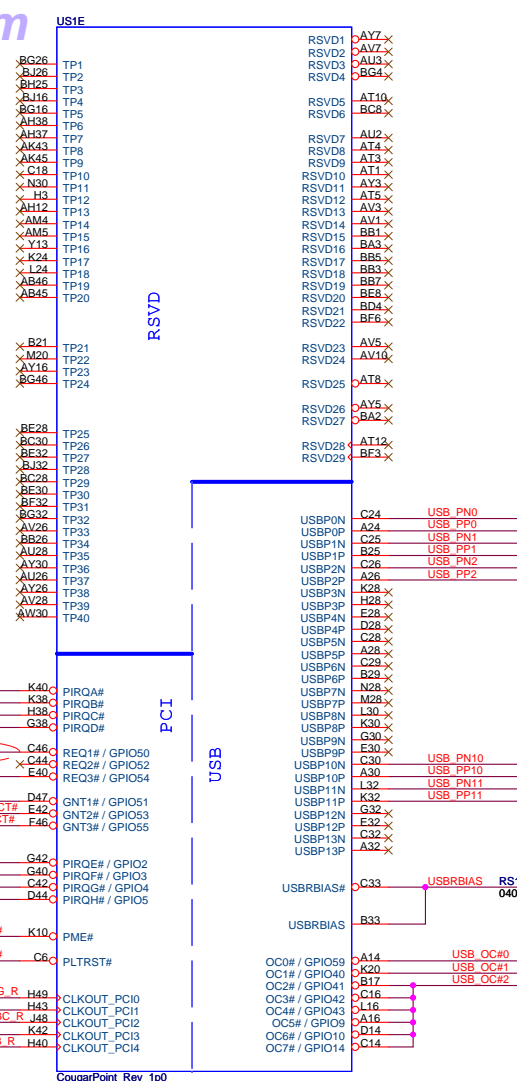
| BBS_BIT1 | BBS_BIT0 | Boot BIOS Location |
|----------|----------|--------------------|
| 0        | 0        | LPC                |
| 0        | 1        | Reserved (NAND)    |
| 1        | 0        | PCI                |
| 1        | 1        | SPI                |



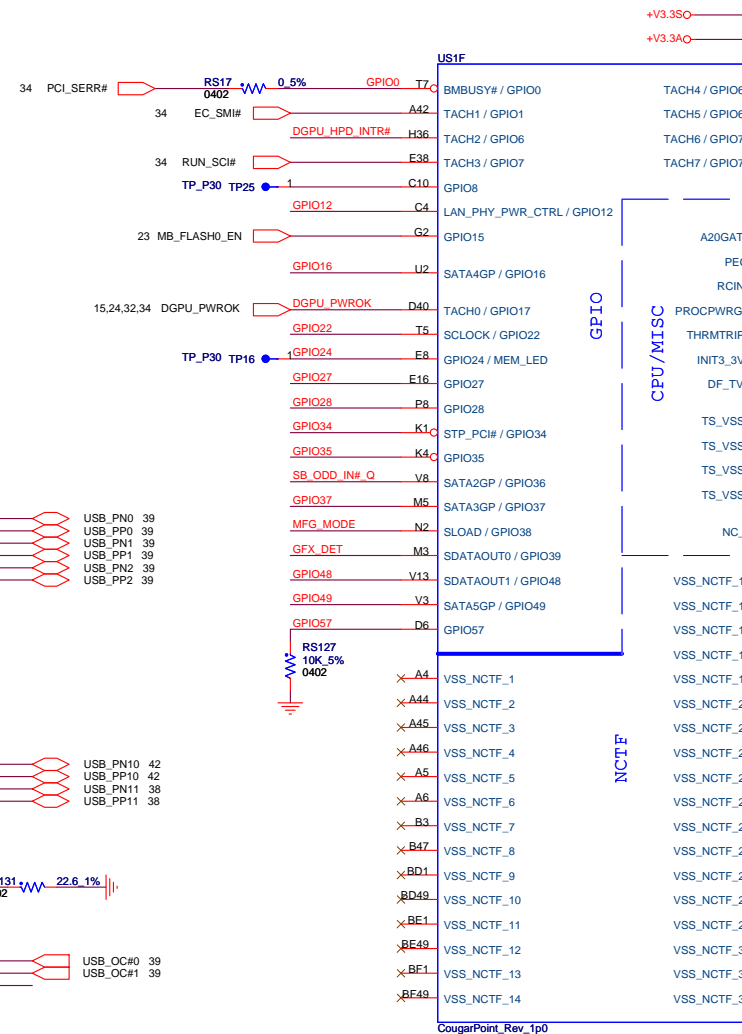
Del RS121 8.2Kohm to +V3.3S  
0820 Update



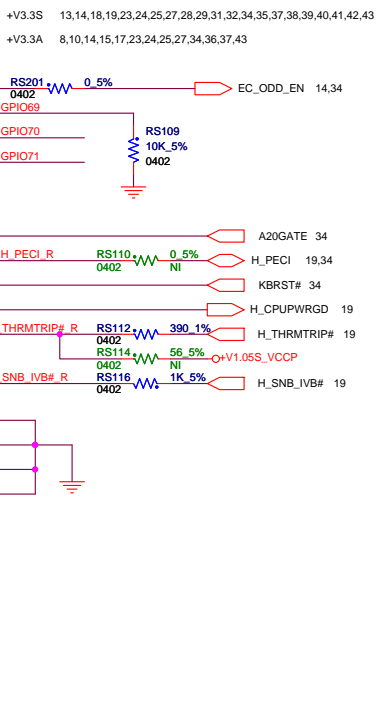
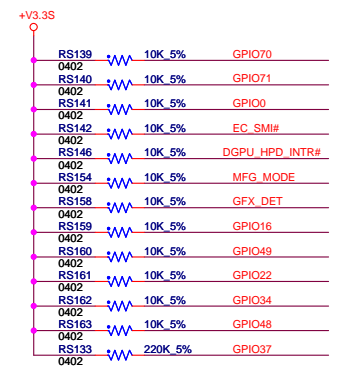
```
02/24 Modify
same as the PV build
```



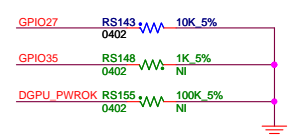
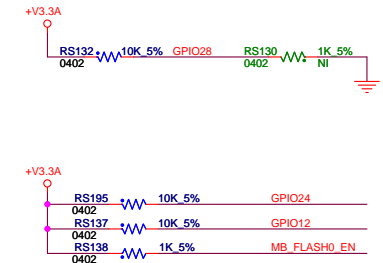
Modify CS102/CS103 to non-stuff on 01/11

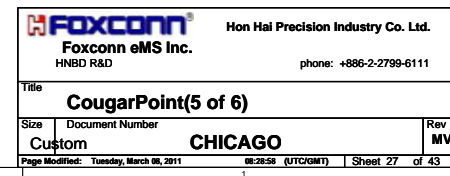


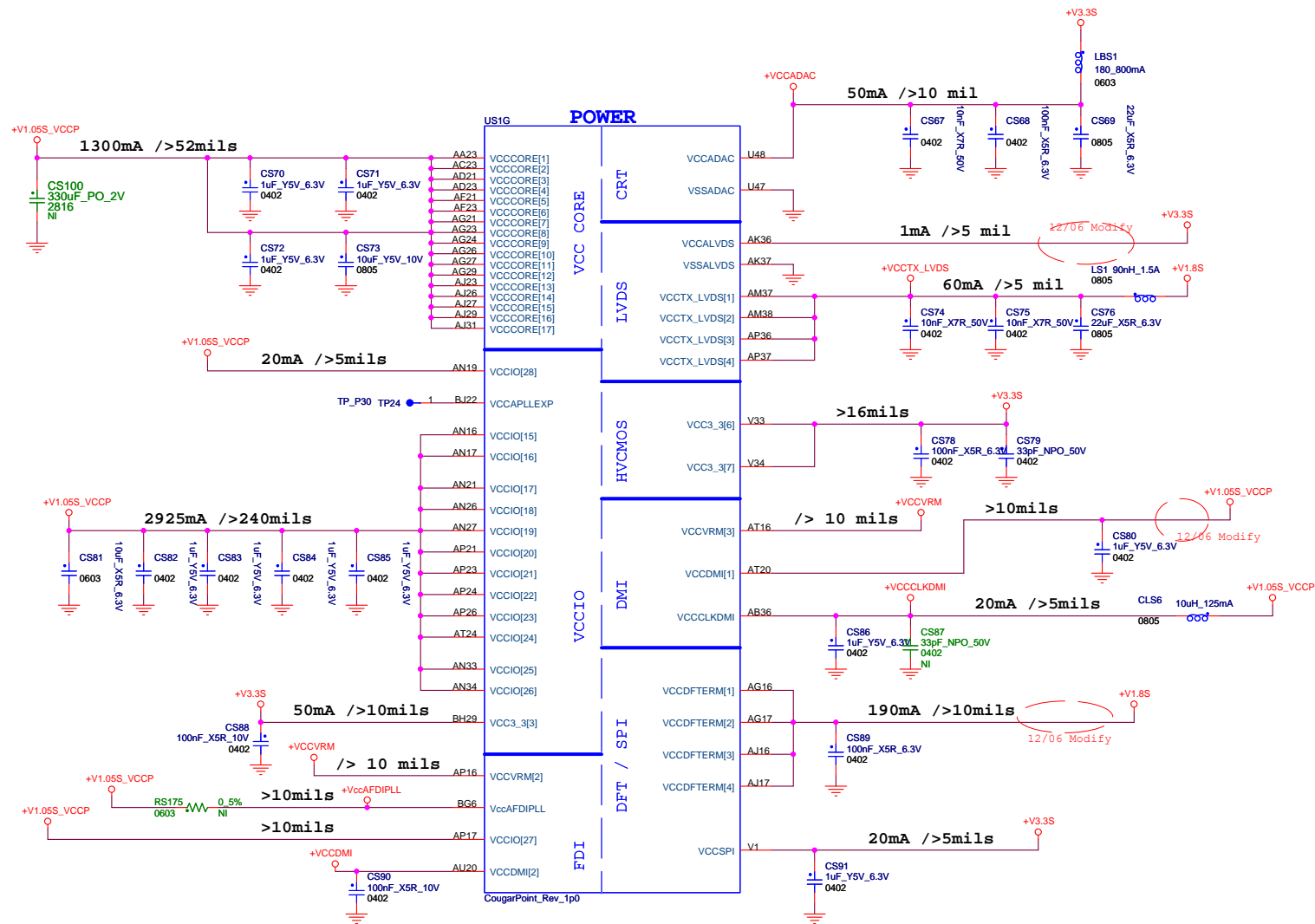
| USB PORT | Function | OC#  |
|----------|----------|------|
| PORT-0   | USB Port | OC0# |
| PORT-1   | USB Port |      |
| PORT-2   | USB Port | OC1# |
| PORT-3   | NC       |      |
| PORT-4   | NC       |      |
| PORT-5   | NC       |      |
| PORT-6   | NC       |      |
| PORT-7   | NC       |      |
| PORT-8   | NC       |      |
| PORT-9   | NC       |      |
| PORT-10  | Camera   |      |
| PORT-11  | WLAN/BT  |      |
| PORT-12  | NC       |      |
| PORT-13  | NC       |      |

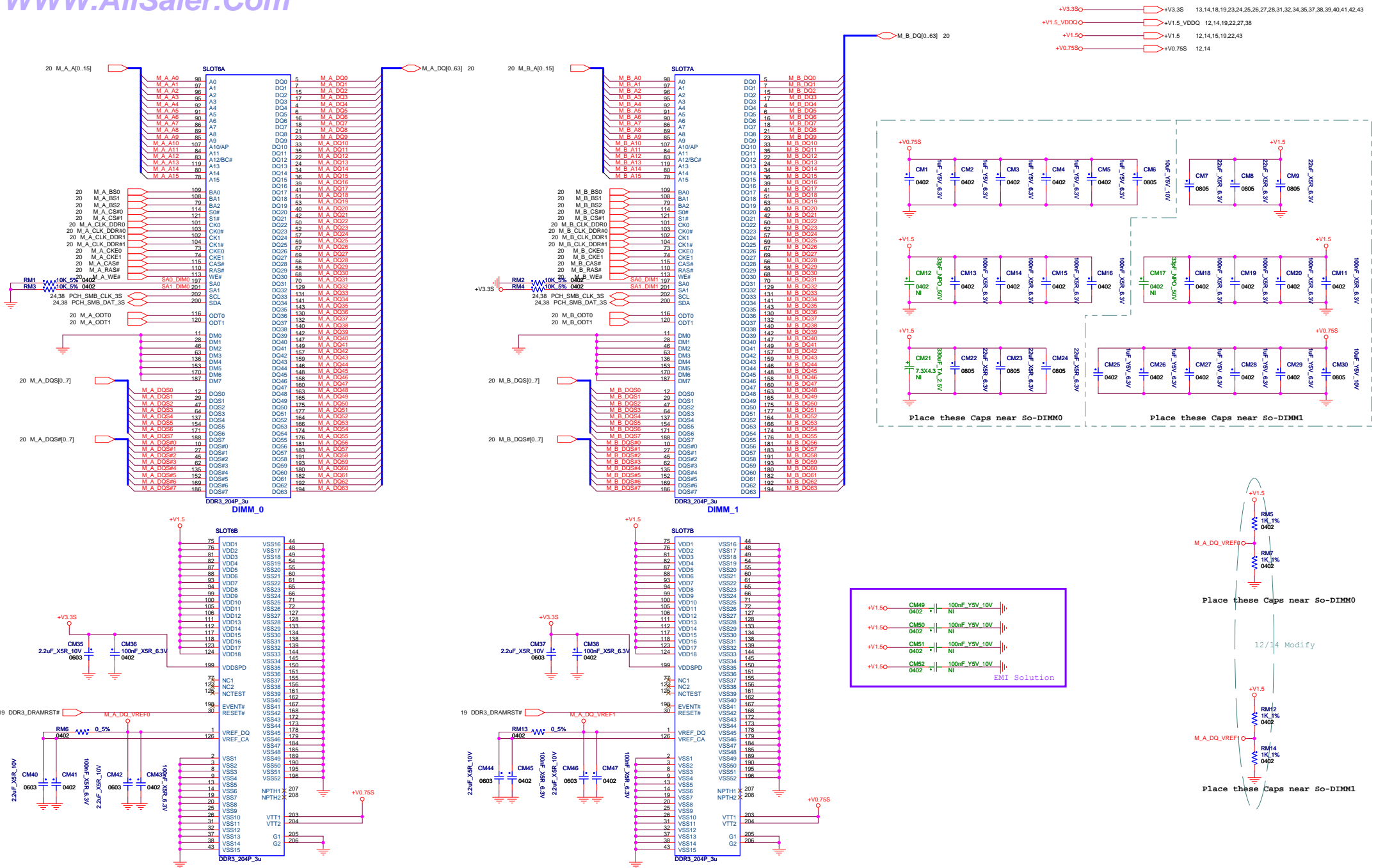


|                      |   |                  |
|----------------------|---|------------------|
| PLL ON DIE VR ENABLE |   |                  |
| GP28                 | 0 | disable          |
|                      | 1 | Enable (Default) |





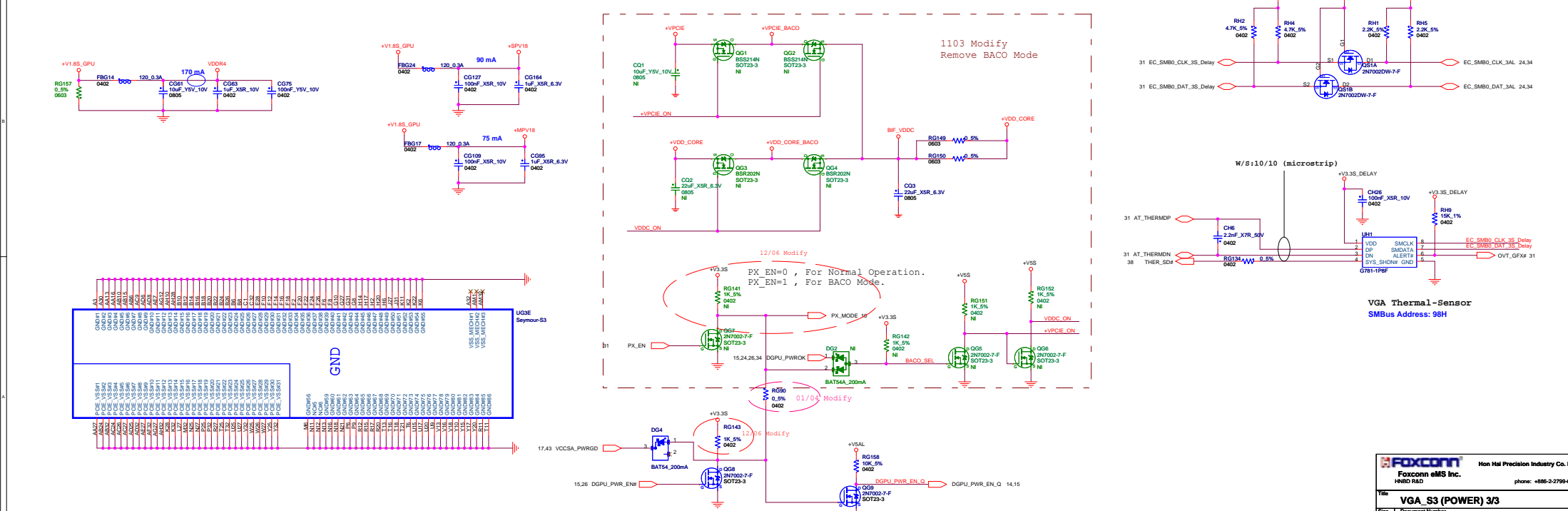
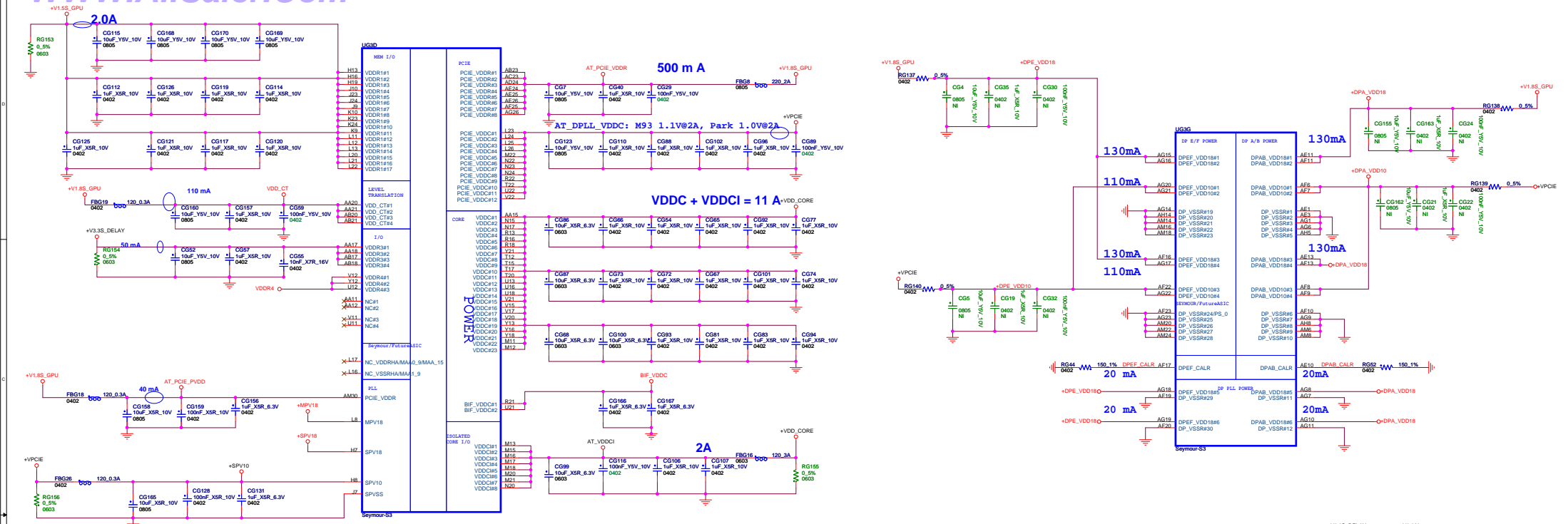








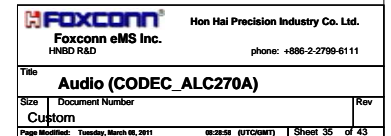


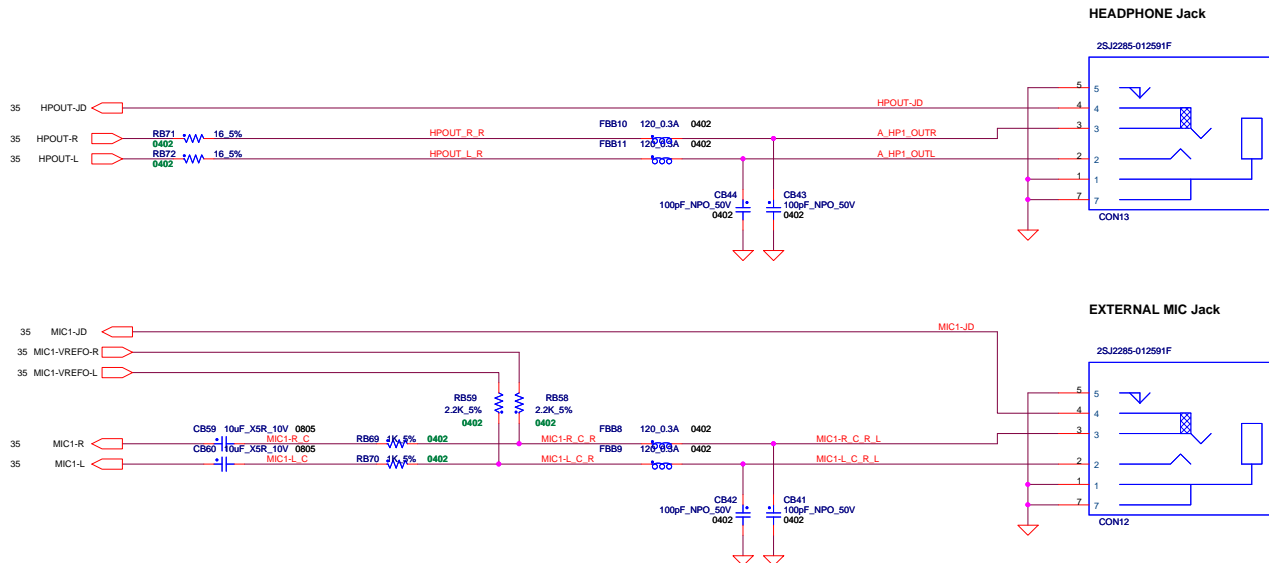
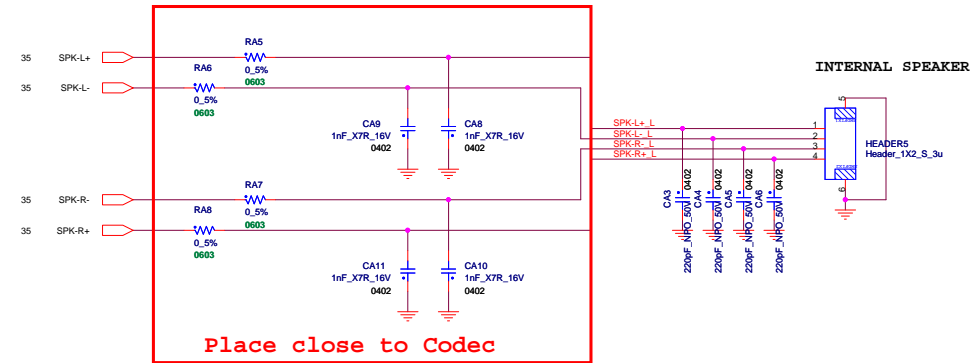
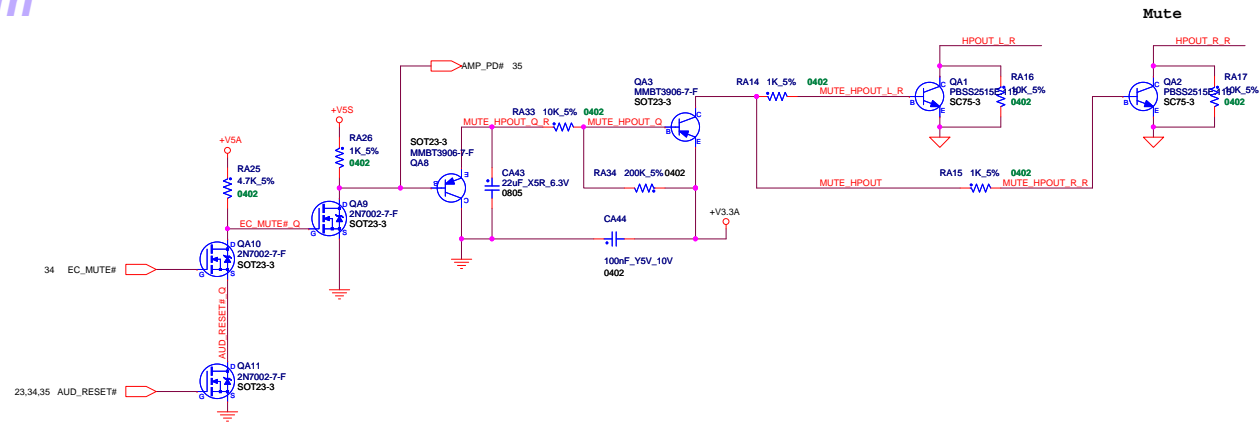


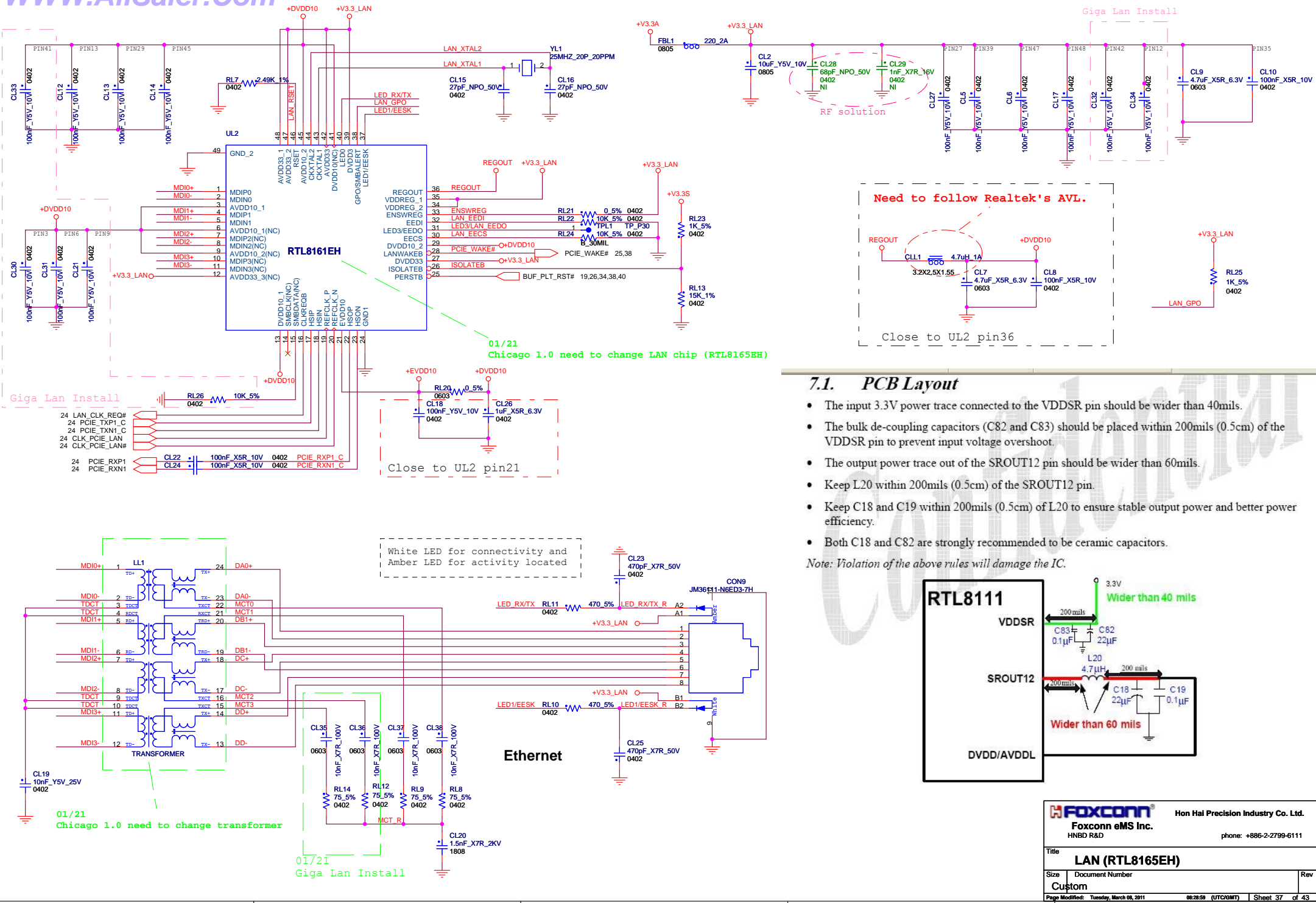








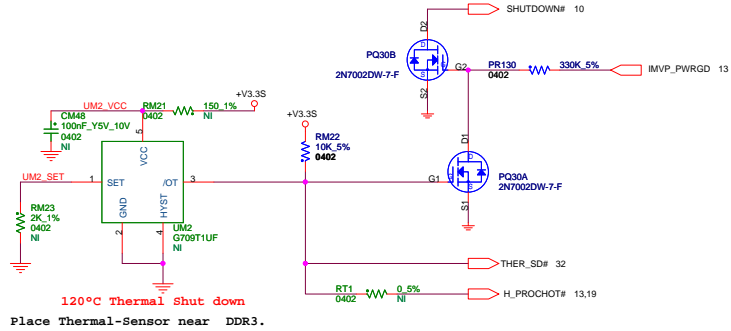
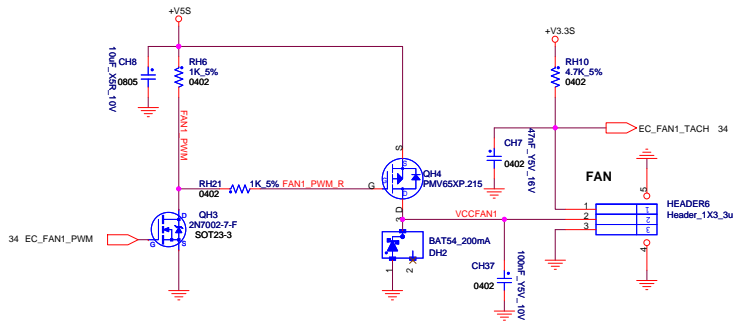
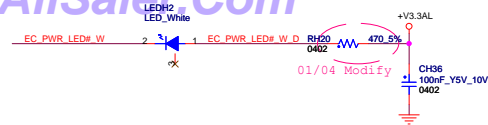




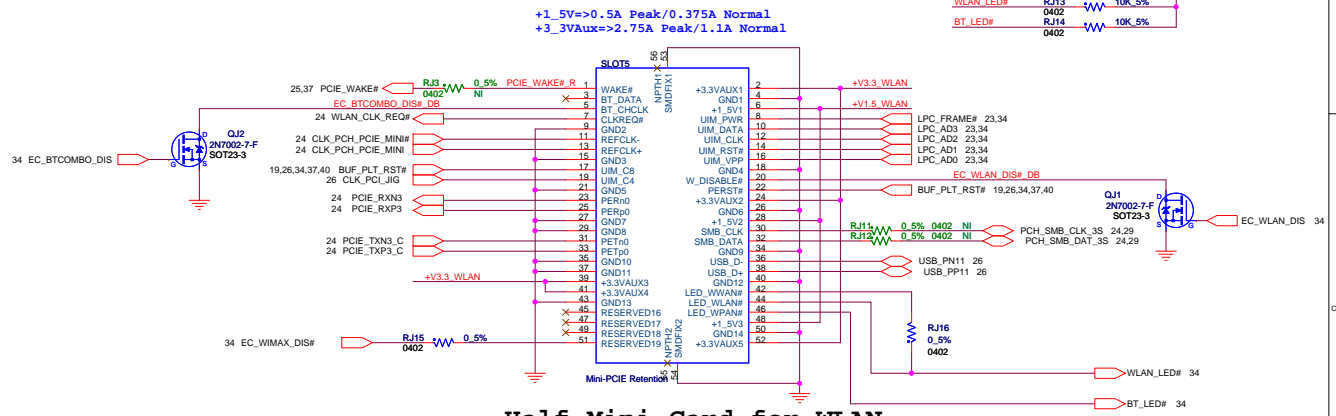
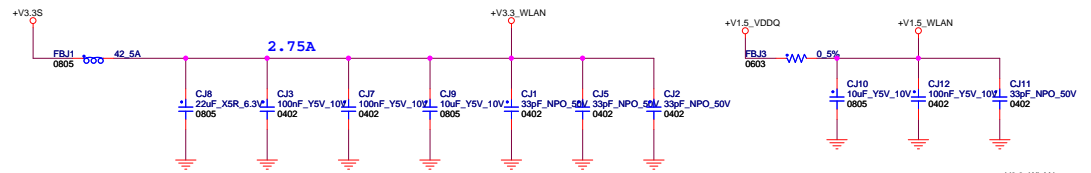
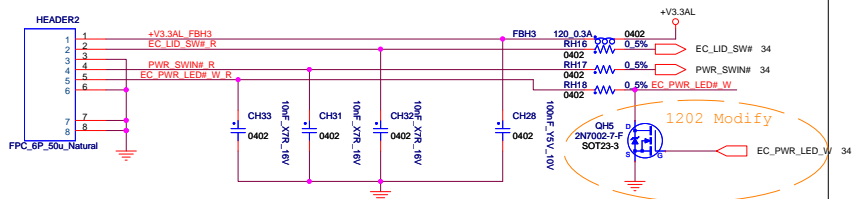
## 7.1. PCB Layout

- The input 3.3V power trace connected to the VDDSR pin should be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200mils (0.5cm) of the VDDSR pin to prevent input voltage overshoot.
- The output power trace out of the SROUT12 pin should be wider than 60mils.
- Keep L20 within 200mils (0.5cm) of the SROUT12 pin.
- Keep C18 and C19 within 200mils (0.5cm) of L20 to ensure stable output power and better power efficiency.
- Both C18 and C82 are strongly recommended to be ceramic capacitors.

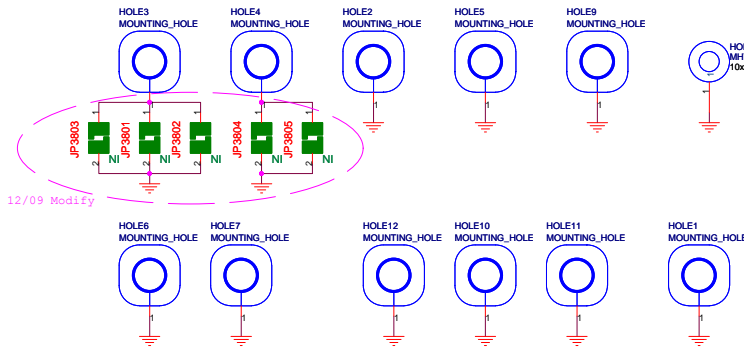
Note: Violation of the above rules will damage the IC.



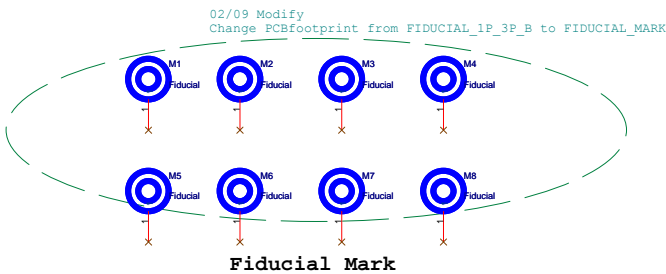
## PWR Board CONN.



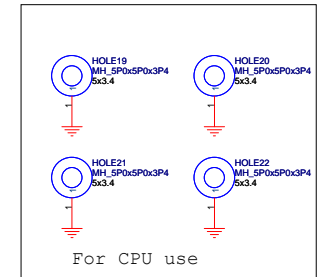
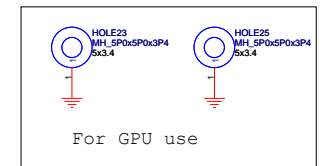
## Half Mini Card for WLAN

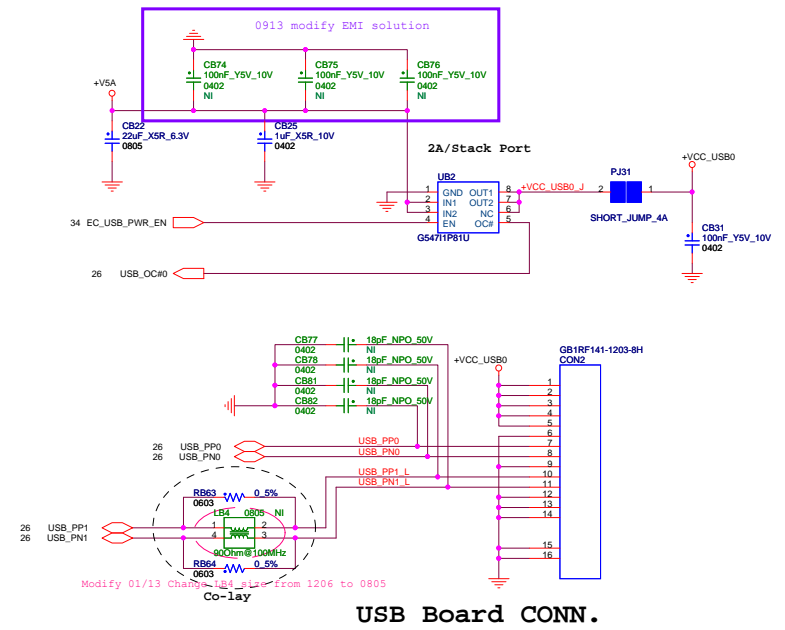
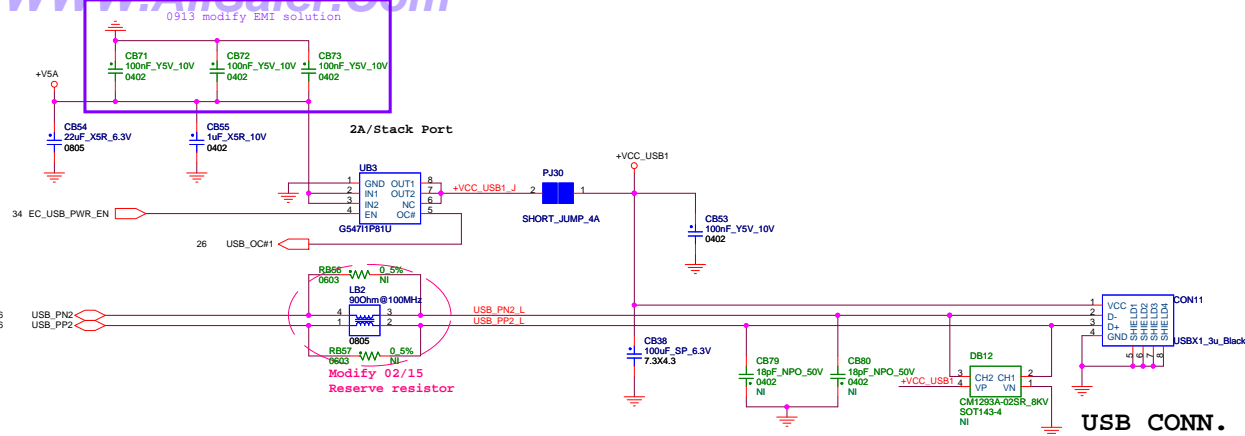


## Mounting HOLE

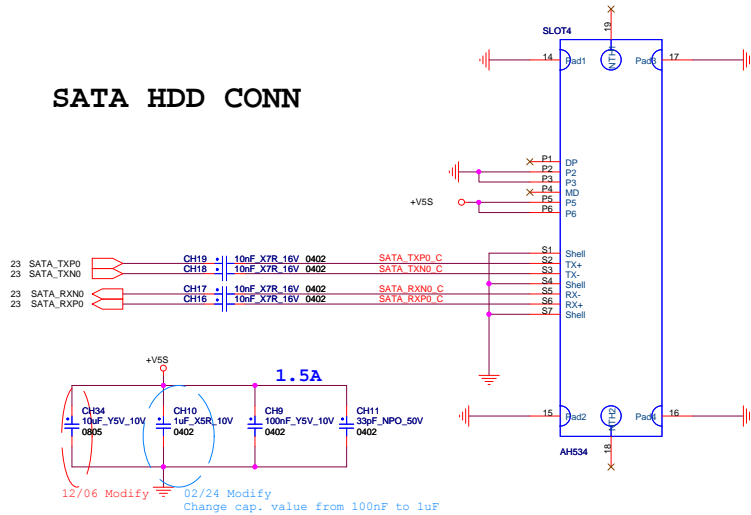


## Fiducial Mark

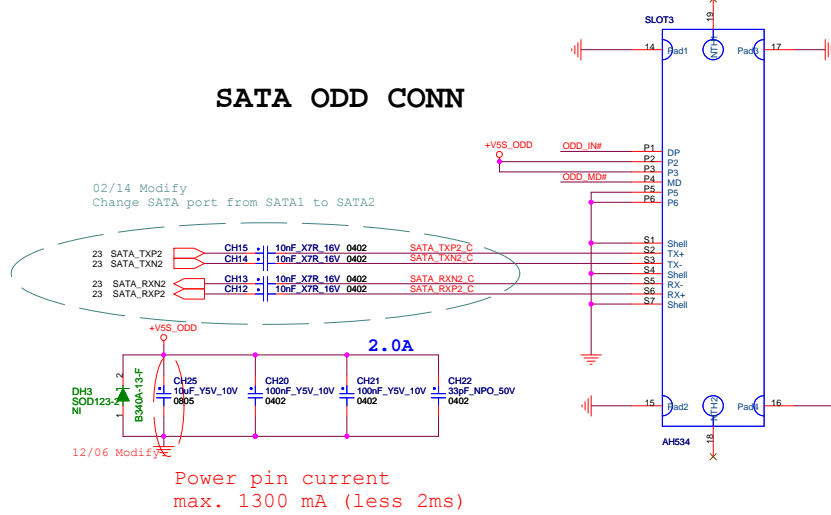




## SATA HDD CONN



## SATA ODD CONN



## HDD/ODD Status LED

